

NOT FOR PUBLICATION

**UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF NEW JERSEY**

MOSAID TECHNOLOGIES INCORPORATED,

Plaintiff,

v.

**SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA, INC.,
SAMSUNG SEMICONDUCTOR, INC., and
SAMSUNG AUSTIN SEMICONDUCTOR, L.P.,**

Defendants.

**INFINEON TECHNOLOGIES NORTH AMERICA
CORP.,**

Plaintiff,

v.

MOSAID TECHNOLOGIES INCORPORATED,

Defendant.

MOSAID TECHNOLOGIES INCORPORATED,

Counterclaimant,

v.

**INFINEON TECHNOLOGIES NORTH AMERICA
CORP., INFINEON TECHNOLOGIES AG,
INFINEON TECHNOLOGIES HOLDING NORTH
AMERICA CORP., and INFINEON
TECHNOLOGIES RICHMOND LLP,**

Counterdefendants.

01-CV-4340 (WJM)

OPINION

HON. WILLIAM J. MARTINI

03-CV-4698 (WJM)

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MARTINI, U.S.D.J.:

On September 12, 2001, plaintiff MOSAID Technologies Incorporated
("MOSAID") filed this patent infringement action against Samsung Electronics Co., Ltd., et al.,¹

¹MOSAID's original complaint listed Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. as defendants. MOSAID later amended its complaint to include Samsung Austin Semiconductor, L.P. as a defendant. Collectively, they will be referred to as "Samsung."

alleging infringement of seven patents. These patents generally claim circuits on dynamic random access memory (“DRAM”) chips.

In early 2003, the Court established a briefing schedule for the parties’ claim construction briefs. Before the briefs were due, the parties requested, and the Court granted, an extension of the page limitation, from 40 to 100 pages, so that the parties could fully address the large number of disputed claim terms. MOSAID and Samsung then briefed their proposed constructions for 63 claim terms.

As this case neared a *Markman* hearing, a similar patent action involving MOSAID was proceeding in the Northern District of California. In that action, Infineon Technologies North America Corp. had filed a declaratory judgment patent action against MOSAID. MOSAID counterclaimed, alleging that Infineon North America Corp., et al., were infringing the same seven patents asserted against Samsung.² Infineon sought an order from the Judicial Panel on Multidistrict Litigation to centralize the MOSAID DRAM chip patent cases in the Northern District of California. On September 15, 2003, after considering the parties’ arguments, the panel determined that centralization of the claims in this Court would promote judicial economy, and so ordered the transfer of the California action to this Court where it subsequently was consolidated with the Samsung action.

Since Infineon had not participated in the already completed *Markman* briefing schedule, the Magistrate Judge handling pretrial matters scheduled another round of claim

²In its counterclaims, MOSAID named as defendants Infineon Technologies North America Corp., Infineon Technologies AG, Infineon Technologies Holding North America Corp., and Infineon Technologies Richmond LLP. Collectively, they will be referred to as “Infineon.”

construction briefing. This new schedule required Infineon to file the initial claim construction brief, MOSAID to file an opposition brief, and both Infineon and Samsung to file reply briefs. Once again, the parties exceeded the page limit of 40 pages to address most of the disputed claim terms.

At around the time the new briefing schedule was established, the Magistrate Judge also permitted MOSAID to amend its infringement claims against Infineon and Samsung to include two additional patents, thus bringing the total number of allegedly infringed patents to nine. The addition of these two patent did not however, affect the number of claim terms in dispute for the *Markman* hearing.

During the second briefing period, Infineon submitted proposed constructions for two new terms, bringing the number of disputed claim terms to 65. As the *Markman* hearing neared, the parties whittled the number of disputed terms down to 30. The dispute concerning those 30 terms shifted, and in most cases narrowed, as the parties continued to submit revised claim constructions up until the day before the *Markman* hearing. On January 27 and 30, 2004, the Court conducted the *Markman* hearing concerning those terms.³

The Court, having considered the parties' vast number of submissions, and having heard oral argument for two whole days, construes the 30 disputed claim terms as set forth below.

³At the start of the *Markman* hearing on January 27, 2004, the parties jointly submitted a chart that set forth the agreed upon meaning of 22 claim terms. (1/27/04 Chart entitled "Agreed and Partially Agreed Claim Terms"). This Court adopts the agreed upon meanings for those claim terms as fully set forth in the Conclusion, *infra*.

BACKGROUND

I. Overview

The subject matter of the nine patents involved in this litigation concerns circuitry in DRAM chips. The nine patents involved in this case can be broken down into two main groups. The first group, consisting of five patents, will be referred to as the “Lines patents” because they all name Ms. Valerie Lines as the sole inventor. The Lines patents are: U.S. Patent No. 5,214,602 (“the ‘602 patent”), U.S. Patent No. 5,751,643 (“the ‘643 patent”), U.S. Patent No. 5,822,253 (“the ‘253 patent”), U.S. Patent No. 6,278,640 (“the ‘640 patent”), and U.S. Patent No. 6,603,703 B2 (“the ‘703 patent”). The Lines patents are directed towards word line driver circuitry that applies a regulated, boosted voltage to a word line in a DRAM chip. All of these patents derive from a common application, Application No. 680,746, filed on April 5, 1991.

The second group of patents will be referred to as the “Foss patents” because each of the four patents names Mr. Richard Foss as the first of several inventors.⁴ The Foss patents are: U.S. Patent No. 5,828,620 (“the ‘620 patent”), U.S. Patent No. 6,055,201 (“the ‘201 patent”), U.S. Patent No. 6,236,581 B1, and U.S. Patent No. 6,850,654 B2. The Foss patents are directed towards voltage pumps, or Foss pumps as they will later be referred to, that “pump” up a supply voltage to a boosted level, which can then be applied to the word line by using a circuit such as the Lines invention. All of these patents derive from a common application, Application No. 680,994, filed on April 5, 1991.

Before addressing the patents in suit, it is important to have a basic understanding of how a DRAM chip works. A DRAM chip enables an electronic device, such as a computer, to

⁴Ms. Lines is also one of the named inventors of the Foss patents.

store information temporarily without having to save it to a permanent storage device, *e.g.*, a hard drive. A DRAM chip is commonly composed of hundreds of millions of memory cells. These memory cells are arranged in a two dimensional array of columns and rows. Each memory cell contains a storage capacitor and an access transistor. *See* '602 patent, Fig. 1. Each memory cell is limited in its ability to retain information; it can only store information in discrete binary values, *i.e.*, ones and zeroes. A "one" is stored as an electrical charge above a certain value, *e.g.*, V_{dd} . A "zero" is stored as an electrical charge below a certain value, *e.g.*, V_{ss} , ground or zero volts. The binary value is stored in the storage capacitor in the form of an electric charge, usually referred to as a voltage.

The access transistor acts as a switch that determines whether an electric charge flows to or from the storage capacitor. In DRAM chips, all access transistors are metal-oxide semiconductor ("MOS") transistors, also referred to as field effect transistors ("FETs"). All MOS transistors have three terminals: source, drain and gate.⁵ Each terminal can receive a voltage. The gate functions as the switch. The voltage that is applied to the gate determines whether and how much current passes between the drain and the source.

There are two types of MOS transistors: n-channel MOS transistors (also referred to as N-MOS or N-FET transistors) and p-channel MOS transistors (also referred to as P-MOS or P-FET transistors).⁶ There are two important differences between these types of transistors when

⁵An illustration of a transistor can be seen in Figure 1 of the Lines patents. *See, e.g.*, '602 patent, Fig. 1. Element 3A is a memory cell access transistor. Its gate is connected to the word line; its drain is connected to the bit line; and its source is connected to element 4A, which is the memory cell storage capacitor. *Id.*

⁶Both types of transistors are used in the patented circuitry. For example, in Figure 1 of the Lines patents elements 3A and 3B are N-MOS transistors, whereas element 14A is a P-MOS

dealing with positive voltages.⁷ First, the two transistors differ on how they permit voltage to pass between drain and source. In an N-MOS, a positive voltage must be applied to the gate in order to pass a positive voltage from the drain to the source. If zero volts is applied to the gate, no voltage will pass between the drain and the source. A P-MOS works in the exact opposite fashion. In a P-MOS, zero volts or V_{ss} must be applied to the gate in order for a positive voltage to pass from source to drain. If a positive voltage is applied to the gate of a P-MOS transistor, no voltage is allowed to pass.

Second, unlike a P-MOS, in order for an N-MOS transistor to pass the full voltage applied to its drain, the full voltage plus some additional threshold voltage (V_{tn}) must be applied to the gate.⁸ For example, in order for an N-MOS transistor to pass a full voltage V_{dd} from source to drain, V_{dd} plus V_{tn} must be applied to the gate. Thus, when passing a voltage V_{dd} from drain to source, the highest voltage on the N-MOS transistor will be equal to or exceed V_{dd} plus V_{tn} . The voltage V_{dd} plus V_{tn} is known as a boosted voltage because V_{dd} has been boosted by V_{tn} . In contrast, a P-MOS transistor passing a positive voltage does not lose a threshold voltage. For

transistor. *See, e.g.*, '602 patent, Fig. 1. Graphically, the distinction between the two transistors is made by a circle at the gate of a P-MOS transistor.

⁷Although it was brought to the Court's attention during the *Markman* hearing that negative voltages may be used in a circuit, throughout this opinion, the Court assumes that positive voltages are being used in the DRAM chip because it does not materially affect the Court's analysis.

⁸When an N-MOS transistor passes a positive voltage, it suffers a threshold voltage loss. If a positive voltage applied to the gate of an N-MOS transistor does not exceed V_{tn} , no voltage will pass through the transistor. Only when a voltage above V_{tn} is applied to the gate, will voltage begin to flow through the transistor, and even then the voltage that flows through will be the voltage at the gate minus V_{tn} . Thus, in order to pass a full V_{dd} from the drain to the source, a voltage equal to at least V_{dd} plus V_{tn} must be applied to the gate.

example, in order to pass the full voltage V_{dd} from source to drain, zero volts must be applied to the gate of the P-MOS transistor. Thus, a P-MOS transistor does not need a boosted voltage to pass the full voltage at its source.

Each memory cell access transistor is an N-MOS transistor. *See, e.g.*, '602 patent, Fig. 1. As discussed earlier, the gate of each transistor is connected to a word line, the drain of each transistor is connected to a bit line, and the source of each transistor is connected to a storage capacitor. *Id.* The word line and bit line are used to write information into and read information out of the storage capacitor. The bit line transfers the bit of information as a voltage to and from the storage capacitor through the access transistor. The word line applies a voltage to the gate of the access transistor in order to allow voltages (or information) to transfer into and out of the storage capacitor. Since the access transistor is an N-MOS transistor, in order to write a voltage V_{dd} from the bit line to the storage capacitor, the word line voltage must apply a boosted voltage V_{pp} ⁹ to the gate of the access transistor.

In order to apply a voltage V_{pp} to the word line, circuitry outside the memory cell must boost the voltage V_{dd} to a V_{pp} voltage level. Whether that boosted voltage is applied to the word line is determined in part by a "pass transistor." When other circuitry sends the pass transistor the appropriate signal, the pass transistor applies the voltage V_{pp} to the word line, thus activating the memory cell access transistor connected to the word line.

A pass transistor can be either an N-MOS or P-MOS transistor. The type of transistor used as the pass transistor determines what voltage must be applied to its gate to allow a full V_{pp} to pass through the transistor. If a P-MOS transistor is used, the full V_{pp} transfers from

⁹ V_{pp} is a voltage that equals at least V_{dd} plus V_{tn} . '602 patent, col. 2, ll. 44-46.

the source to the drain when zero volts is applied to the gate. If an N-MOS transistor is used, due to the threshold voltage loss, the voltage applied to the gate must be boosted by an additional V_{tn} to pass the full V_{pp} . Thus, in order to pass a full V_{pp} , the gate voltage has to exceed V_{pp} plus V_{tn} , which must be greater than V_{dd} plus $2V_{tn}$.

II. Detailed Description

In the prior art, word line driver circuitry, which determined when and how to apply a boosted voltage V_{pp} to the word line, suffered from two problems. First, the prior art circuits used N-MOS transistors as the pass transistor, which generated unacceptably high voltages and reduced the reliability of the DRAM chips. '602 patent, col. 1, ll. 33-54. As explained earlier, in order to pass a full voltage V_{dd} plus V_{tn} to the word line, the gate voltage of an N-MOS transistor has to exceed V_{dd} plus $2V_{tn}$. '620 patent, col. 2, ll. 30-35. In order to achieve this higher voltage on the gate, the N-MOS transistors would perform a technique called "self-bootstrapping."

Generally speaking, self-bootstrapping requires a voltage, usually at least V_{dd} , to be applied to the gate of the transistor before any voltage is applied to the drain. This creates a voltage difference between the gate and drain/source that the transistor will attempt to maintain. For example, if V_{dd} is applied to the gate and the drain is at zero volts, the transistor will try to maintain the voltage difference, V_{dd} , even when a voltage is applied to the drain. Thus, when the boosted voltage V_{pp} arrives at the drain, the transistor will self-bootstrap by boosting the voltage on the gate by V_{pp} , resulting in a voltage at the gate of V_{pp} plus V_{dd} . The voltage at the gate now

substantially exceeds V_{pp} ,¹⁰ and consequently, the pass transistor will apply the full V_{pp} to the word line. The problem with this technique is that the self-bootstrap voltage at the gate of the transistor could “exceed the tolerable voltages in the memory, thus adversely affecting reliability.” ‘602 patent, col. 1, ll. 52-53.

Second, the prior art applied “uncontrolled” voltages¹¹ to the word line, affecting the voltage applied to the gate of the access transistor, and potentially affecting the voltage level that was stored in the storage capacitor. To ensure that a full logic “one” was stored in the storage capacitor, the prior art raised the uncontrolled voltage level applied to the word line well above V_{dd} plus V_{tn} . Like the high voltages on the self-bootstrapping transistor, these high voltages on the memory cell access transistors made the DRAM chips less reliable:

Since memory voltage tolerances vary from memory to memory, since the temperature environment in which the memory is placed and which it endures with different current conduction levels vary, since power supplies for various devices do not provide constant, precise and stable voltages, the prior art techniques of driving the word line to very high voltages in order to reliably overcome N-channel FET thresholds in the face of such variation and to speed up operation has been found to cause random failures of memory. Appl. No. 07/680,746, 2/13/92 Response to PTO Action at p. 8.

¹⁰See ‘602 patent, col. 2, ll. 37-42.

¹¹An uncontrolled voltage is a voltage that may vary considerably over time, as opposed to a substantially constant voltage. In the prior art, an uncontrolled voltage was created by inserting a boosting capacitor between the pass transistor and the word line. See Appl. No. 07/680,746, 2/13/92 Response to PTO Action at pp. 7-11 (discussing the prior art reference Tran and its use of a boosting capacitor). This would result in a “word line voltage that increases over a period [of time].” *Id.* at 9.

The inventors of the Lines and Foss patents devised circuits that eliminate these problems. The inventors of the Foss patents devised a voltage pump that can take a supply voltage, *e.g.*, V_{dd} , and boost it to a controlled voltage V_{pp} . Ms. Lines then invented circuits that take a controlled voltage V_{pp} from a circuit such as the Foss pump and apply it to the word line without using circuits that generate uncontrolled high voltages and dangerous bootstrap voltages. Together, the Lines and Foss patents eliminate the prior art's reliability problems by keeping the voltage levels below that which damages the access and pass transistors.

DISCUSSION

I. The Law of Claim Construction

Claim construction is a matter of law reserved for the Court to decide. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996). Claim construction analysis begins with and remains focused on the language of the claims because it is that language the patentee purposefully chose to “particularly point[] out and distinctly claim[] the subject matter which the patentee regards as his invention.” *Texas Digital Sys., Inc. v. Telegenix, Inc.*, 308 F.3d 1193, 1201-02 (Fed. Cir. 2002) (quoting 35 U.S.C. § 112 ¶ 2). Because the words used in the claims are viewed from the perspective of one of ordinary skill in the art, the words bear a “heavy presumption” that they take on their ordinary meaning, unless the patentee evinced an intent to deviate from that meaning. *Id.* at 1202; *Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1298 (Fed. Cir. 2003).

In order to determine the ordinary meaning of claim terms, the Court may look to the intrinsic evidence, *i.e.*, the claims themselves, the specification and prosecution history, and

dictionaries and treatises. *Texas Digital*, 308 F.3d at 1202; *Brookhill-Wilk*, 334 F.3d at 1298.

When looking at the language of the claims, the Court must not only consider the claim terms in dispute, but their surrounding context as well. *Brookhill-Wilk*, 334 F.3d at 1299. Dictionaries and treatises, although helpful to determine the ordinary meaning of claim terms, must be used carefully. Since the ordinary meaning of words may change over time, the Court must limit its analysis to dictionaries and treatises that are informative of the ordinary meaning of the claim terms as of the time the patent issued. *Brookhill-Wilk*, 334 F.3d at 1299 (The references “are not contemporaneous with the patent, do not reflect the meanings that would have been attributed to the words in dispute by persons of ordinary skill in the art as of the grant of the ‘003 patent, and for those reasons are not considered in our . . . claim construction analysis.”). Further, when attempting to ascertain the ordinary meaning of technical words, the Court must be circumspect about consulting general purpose dictionaries. *See, e.g., Inverness Med. Switzerland GmbH v. Princeton Biomeditech Corp.*, 309 F.3d 1365, 1369-70 (Fed. Cir. 2002). Finally, “[i]f more than one dictionary definition is consistent with the use of the words in the intrinsic record, the claim terms may be construed to encompass all such consistent meanings.” *Texas Digital*, 308 F.3d at 1203.

The specification and prosecution history must always be examined as part of the claim construction analysis to determine whether the presumption of ordinary meaning is rebutted.¹² *Brookhill-Wilk*, 334 F.3d at 1298. First, the “presumption will be overcome where the patentee, acting as his or her own lexicographer, has clearly set forth a definition of the term

¹²In addition, if there are multiple, conflicting dictionary definitions, the Court must consult the specification and prosecution history to determine that definition which is “most consistent with the use of the words by the inventor.” *Texas Digital*, 308 F.3d at 1203.

different from its ordinary and customary meaning.” *Id.* at 1299; *Texas Digital*, 308 F.3d at 1204 (“Indeed, the intrinsic record may show that the specification uses the words in a manner clearly inconsistent with the ordinary meaning reflected, for example, in a dictionary definition. In such a case, the inconsistent dictionary definition must be rejected.”). Second, the presumption will be overcome where a patentee disclaims or disavows claim scope “by using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope.” *Brookhill-Wilk*, 334 F.3d at 1299; *Texas Digital*, 308 F.3d at 1204. “Last, as a matter of statutory authority, a claim term will cover nothing more than the corresponding structure or step disclosed in the specification, as well as equivalents thereto, if the patentee phrased the claim in step- or means-plus-function format.” *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1367 (Fed. Cir. 2002) (citing 35 U.S.C. § 112 ¶ 6).

If the ordinary meaning can be ascertained from the intrinsic evidence and contemporaneous dictionaries and treatises, the Court need not look to the extrinsic evidence as part of its obligation to construe the disputed claim terms. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996).

II. The Disputed Claim Terms

1. “ V_{dd} ”

The central dispute surrounding the claim term “ V_{dd} ” concerns whether it is limited to an externally supplied voltage applied to a pin of the DRAM, or whether it can also include an internally supplied, or “on-chip,” voltage. This distinction is significant because a DRAM chip may use the externally applied voltage in one of two ways. First, a DRAM chip

may use an externally applied voltage, *e.g.*, 5 volts, in some circuits on the chip without any manipulation. Second, a DRAM chip may reduce, referred to as “stepping down” or “down converting,” the externally applied voltage to a lesser voltage and use that lesser voltage in some circuits on the chip. For example, an externally applied voltage of 5 volts may be stepped down to 3.3 volts, which is then used in certain circuits on the chip. Defendants contend that “ V_{dd} ” does not include any stepped down voltages that may be used on the chip. MOSAID contends that “ V_{dd} ” should not be limited to an external voltage, but may also include stepped down voltages.

Claim construction analysis begins by determining whether the claim term has an ordinary meaning. To that end, one first looks to the language of the claims.¹³ The claims of the ‘602 patent do not explicitly limit “ V_{dd} ” to an externally applied voltage. For example, claim 1 of the ‘602 patent states:

1. A dynamic random access memory (DRAM) comprising bit lines and word lines, memory cells connected to the bit lines and word lines, each memory cell being comprised of an access field effect transistor (FET) having its source-drain circuit connected between a bit line and *a high logic level voltage V_{dd} bit charge storage capacitor*, the field effect transistor having a gate connected to a corresponding word line;

a high V_{pp} supply voltage source which is in excess of high logic level voltage V_{dd} plus one transistor threshold voltage;

¹³The parties agreed that all of the disputed claim terms have the same meaning regardless of what patent they appear in. Consequently, as a matter of convenience when dealing with the 9 patents in suit, for each disputed claim term, the Court began by looking at the term in the context of the first patent that issued from the Patent Office. To the extent that the parties felt it was necessary, they were encouraged to direct the Court to other locations in other patents where the context of the claim term may shed light on its meaning. Accordingly, although certain claim terms may only be addressed in the context of one patent, they were considered in the context of all of the patents in suit.

means for selecting the word line and means having an input driven by the selecting means for applying the V_{pp} supply voltage level directly to the word line through the source-drain circuit of an FET. '602 patent, claim 1 (emphasis added).

Claim 1, like the other '602 claims, says nothing about " V_{dd} " being an externally applied voltage.

Instead, the claim speaks of " V_{dd} " as a voltage level that the memory cell capacitor can store.

Thus, looking solely at the claim language, " V_{dd} " is not limited to an external voltage.

The Defendants do not dispute the plain language of the '602 claims. Instead, they point to claims 1 and 2 of the '703 patent to support their construction that " V_{dd} " should be limited to an externally applied voltage. Claims 1 and 2 of the '703 patent are:

1. A method of selecting a word line in a dynamic random access memory to store a V_{dd} logic level in a memory cell comprising:
 - applying a controlled supply voltage V_{pp} greater than V_{dd} to a level shifter circuit;
 - applying only V_{dd} logic level signals to the level shifter circuit to produce a logic signal having a state at the V_{pp} voltage; and
 - applying the logic signal having the state at the V_{pp} voltage to the word line.

2. A method of selecting a word line in a dynamic random access memory to store a logic level in a memory cell comprising:
 - applying a controlled supply voltage V_{pp} , greater than the voltage stored in the memory cell, to a level shifter circuit;
 - applying only logic signals having a level less than V_{pp} to the level shifter circuit to produce a logic signal having a state at the V_{pp} voltage; and
 - applying the logic signal having the state at the V_{pp} voltage to the word line. '703 patent, claims 1 and 2 (emphasis added).

The Defendants assert that claims 1 and 2 are identical except that claim 1 speaks of "a V_{dd} logic level in a memory cell," whereas claim 2 simply speaks of "a logic level stored in the memory

cell.” According to Defendants, since claims 1 and 2 are independent claims, under the doctrine of claim differentiation, this difference must be significant and must mean that “ V_{dd} ” means something other than a logic level stored in the memory cell, such as an externally applied voltage.

The Defendants’ conclusion, however, is mistaken. The doctrine of claim differentiation does not require that two claims differ in scope. *O.I. Corp. v. Tekmar Co. Inc.*, 115 F.3d 1576, 1582 (Fed. Cir. 1997) (“Although the doctrine of claim differentiation may at times be controlling, construction of claims is not based solely upon the language of other claims; the doctrine cannot alter a definition that is otherwise clear from the claim language, description, and prosecution history.”) But even if it did, in this case, assuming that the two claims are of different scope does nothing to support Defendants’ argument that “ V_{dd} ” should be limited to an externally applied voltage. Significantly, ‘703 claim 2 does not require that the “logic level” stored in the memory cell be the only internal voltage on the chip. Accordingly, the ‘703 claims, like the ‘602 claims, do not limit “ V_{dd} ” to an externally applied voltage.

Dictionaries and treatises may also be informative of a claim term’s ordinary meaning. Only one dictionary definition for “ V_{dd} ” was submitted in this case. The Radio Shack dictionary states in pertinent part:

V_{DD} , V_{SS} , V_{CC} , V_{EE} - In a MOS circuit, the designation of the power-supply terminal serving the drain, source, collector, or emitter. The double subscript refers to the power-supply terminal, while a single subscript references the parameter at the element of a device . . . In CMOS, the term V_{DD} has been adopted as a convention referring to the positive power-supply terminal, although it is actually applied to the source of a p-channel transistor. *Radio Shack Modern Dict. of Elecs.* 794 (5th ed. 1978).

MOSAID submits this definition as evidence that the ordinary meaning of " V_{dd} " includes internal voltages. Defendants contend that the Radio Shack definition supports its narrow construction. Defendants maintain that the definition, by using the word "terminal," indicates to one of skill in the art that V_{dd} is supplied through an external connection. In support of this argument, Defendants submit a dictionary definition for "terminal," which is defined as "an externally available point of connection to one or more electrodes or elements within a device." *IEEE Standard Dict. of Electrical and Electronics Terms* 997 (4th ed. 1988). Defendants point to the word "externally" in that definition as evidence of the correctness of their proposed construction.

The dictionary definitions support a broader construction of " V_{dd} ." The Radio Shack definition of " V_{dd} " does not limit " V_{dd} " to an externally applied voltage. In fact, it suggests that " V_{dd} " can be an internal voltage since it states that V_{dd} can be "applied to the source of a p-channel transistor," and nothing requires that the source of a p-channel transistor be connected to the external pin of a DRAM chip. Likewise, nothing in the definition of terminal requires that V_{dd} be externally applied to the DRAM chip. Although it does contain the word "externally," it does so in the context of external to "elements *within a device*," *i.e.*, elements *within* the DRAM chip. Consequently, the ordinary meaning of " V_{dd} " is "the substantially constant positive source-drain supply voltage in a MOS circuit."

The '602 specification does not alter the ordinary meaning of " V_{dd} ." The '602 specification includes statements about " V_{dd} " such as: the " V_{dd} level on the bit line 2A, 2B etc. is fully transferred to the associated capacitor," '620 col. 2, ll. 28-29; and the "signals at the voltage level V_{dd} are applied to the inputs of NAND gate 5." '620 col. 3, ll. 15-16. Looking at Figure 1, it is clear that the bit lines and NAND gate 5 are internal circuitry of the chip. Therefore, the

voltage being applied to these devices is an internal voltage that is not necessarily limited to an externally applied voltage.

Accordingly, “ V_{dd} ” shall be construed as “the substantially constant positive source-drain supply voltage in a MOS circuit.”

2. “means for applying”

There is no dispute and the Court finds that the claim term “means for applying” set forth in claim 1 of the ‘602 patent is a means-plus-function term governed by 35 U.S.C. § 112 ¶ 6.¹⁴ The first step in construing a means-plus-function limitation is to identify the particular function of the claim limitation. *Budde v. Harley-Davidson, Inc.*, 250 F.3d 1369, 1376 (Fed. Cir. 2001). The second step is to identify the corresponding structure performing that function. *Id.*; *GoLight, Inc. v. Wal-Mart Stores, Inc.*, 355 F.3d 1327, 1334 (Fed. Cir. 2004). “Structure disclosed in the specification is ‘corresponding’ structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim.” *B. Braun Med., Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997).

The parties agree that the function performed by this term is “applying the V_{pp} supply voltage level directly to the word line through the source-drain circuit of an FET.” The

¹⁴35 U.S.C. § 112 ¶ 6 states:

An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

parties also agree that the structure for performing that function includes level shifter 6 and transistor 14A. They do not however agree on whether the structure can include a secondary decoder, or whether a disclaimer of subject matter applies to this claim term.

MOSAID contends that a secondary decoder is identified as structure for performing the claimed function. MOSAID points to the two locations in the '602 specification that refer to the secondary decoder. In Figure 1, voltage line 15, which is attached to the source of 14A, is identified as the "wordline supply V_{pp} or decoded secondary decoder output." '602 patent, Fig. 1. The description of the preferred embodiment states that "[t]he source of pass transistor 14A is connected to V_{pp} or to a secondary decoder output which provides a V_{ss} or V_{pp} level output." '602 patent, col. 2, ll. 63-65.

MOSAID contends that these two references indicate that there are two embodiments to the "means for applying." The first embodiment is where only one word line is assigned to a word line driver. *See, e.g.*, '602 patent, Fig. 1. In that situation, the parties agree that the structure that performs the claimed function is level shifter 6 and transistor 14A. The level shifter 6 receives an output from NAND gate 5, and if appropriate, sends a signal to pass transistor 14A opening the transistor and applying V_{pp} from the "wordline supply V_{pp} " to the word line.

The second embodiment has multiple word lines attached to a single word line driver. In this more complicated circuit, level shifter 6 sends a signal to multiple P-MOS, pass transistors (*e.g.*, transistors 14A, 14B, and 14C) that are attached to their own, unique word line. Unlike the first embodiment, the sources of the pass transistors cannot be connected to a constant V_{pp} supply voltage. If they were, and the level shifter 6 sent the signal that opened the pass

transistors, then all of the attached word lines would carry a V_{pp} voltage. Since only one word line can receive a V_{pp} voltage at any given time, a circuit including a secondary decoder may be used in conjunction with the word line driver to select and apply a voltage to only one word line.

The secondary decoder receives address information and provides a certain output that is shifted to V_{pp} voltage levels, *i.e.*, V_{ss} (ground) or V_{pp} . It then provides V_{ss} or V_{pp} to the pass transistors (14A, 14B and 14C) that have been enabled by level shifter 6. Because only one word line may be driven at any given time, two of those pass transistors must receive V_{ss} , effectively treating those transistors as if they were closed, and the remaining transistor receives V_{pp} , activating that particular word line.

Defendants do not dispute that in the first embodiment, level shifter 6 and transistor 14A apply V_{pp} to the word line. Rather, they argue that the second embodiment is not included within the scope of the patent. And even if it is, Defendants argue that the specification only identifies the secondary decoder as an alternative voltage supply, not as a structure that applies the V_{pp} voltage to the word line.

Plaintiff is correct. The specification links the secondary decoder to the function of applying the voltage to a word line. Based on the specification, there is no doubt that the secondary decoder can be used to apply the voltage V_{pp} to the source of the pass transistor and, ultimately, to the word line. Consequently, the specification adequately ties the secondary decoder to the claimed function.

Further, the undisputed evidence before the Court shows that the second embodiment, including multiple word lines, is within the scope of the patent. “The law is clear that patent documents need not include subject matter that is known in the field of the invention

and is in the prior art, for patents are written for persons experienced in the field of the invention.” *S3 Inc. v. n Vidia Corp.*, 253 F.3d 1364, 1371 (Fed. Cir. 2001). During the *Markman* hearing, MOSAID represented to the Court, and Defendants conceded, that secondary decoders were well known in the art at the time of the Lines patents. (1/30/04 *Markman* Tr. at 245:17-246:15 and 253:3-255:10). It was further known in the art that a secondary decoder could be used in conjunction with a primary decoder (*e.g.*, NAND gate 5) to select one of several word lines. Peter Gillingham et al., *High-Speed Reliability Circuit Design for Megabit DRAM*, 26(8) IEEE Journal of Solid-State Circuits 1171, 1172 Fig. 2 (1991). Accordingly, the ‘602 disclosure combined with the knowledge of one of ordinary skill in the art clearly indicate that the use of a secondary decoder to apply a voltage V_{pp} to one of several word lines is contemplated.

Additionally, even if that evidence is considered borderline, the Court finds that the ‘602 patent’s prosecution history clearly put the public on notice that a secondary decoder could be used to drive more than one word line. Application No. 07/680,746, an application all of the Lines patents derive from, includes a figure that clearly shows a word line driver circuit connected to two word lines, with a dashed line showing the possibility of more. Appl. No. 07/680,746, 6/24/91 Letter Claiming Right of Priority, UK Appl. No. 9007790 at Fig. 2. One of skill in the art reviewing that figure and the ‘602 specification would undoubtedly know that the inventor contemplated the use of a secondary decoder in conjunction with a word line driver circuit to drive more than one word line. Accordingly, the structure for the term “means for applying” includes a secondary decoder.

Defendants further contend that MOSAID, during prosecution of the Lines patents, disclaimed the use of double bootstrapping and the use of voltages that exceed V_{pp} .

MOSAID counters by arguing that there can be no disclaimer because there is no claim language that Defendants can “hook” their disclaimer to, and even if there is, the patentees did not disclaim any subject matter.

MOSAID’s argument that there is no “hook” in the claims is inapt and unsupported by case law. In order for there to be a disclaimer of double bootstrapping, MOSAID would require the claims explicitly state “without double bootstrapping,” or at least contain the word “bootstrap.” MOSAID does not cite to any case law for that proposition, and this Court is not aware of any. Indeed, whether a disclaimer arises is not determined by a verbal “hook,” but by whether a claim term, if construed broadly, reads on subject matter the written description makes clear does not fall within the scope of the patent. *See, e.g., Microsoft Corp. v. Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1346-49 (Fed. Cir. 2004) (concluding that the district court properly limited the terms “sending,” “transmitting,” and “receiving” to the transmission of data over a telephone line connection even though many of the claims did not exclude the transmission of data over a packet-switched network).

As the Federal Circuit stated in *Cultor Corp. v. A.E. Staley Mfg. Co.*, 224 F.3d 1328 (Fed. Cir. 2000), “[c]laims are not correctly construed to cover what was expressly disclaimed. *Id.* at 1331. The reason is quite simple:

The public notice function of a patent and its prosecution history requires that a patentee be held to what he declares during the prosecution of the patent. A patentee may not state during prosecution that the claims do not cover a particular device and then change position and later sue a party who makes that same device for infringement.

Spring Window Fashion LP v. Novo Indus., LP, 323 F.3d 989, 995 (Fed. Cir. 2003).

To the extent that the “means for applying” could include a double bootstrapping circuit, this Court is compelled to determine whether such a disclaimer was made.¹⁵

MOSAID’s argument that no disclaimer was made is belied by the intrinsic evidence and MOSAID’s own admission that “[d]uring prosecution, the applicant distinguished circuits having a boost capacitor connected to the word line (*e.g.*, Tran) and double-bootstrapping circuits (*see, e.g.*, Background to the Invention, Col. 1, ll. 44-54, ‘640 patent). *See* Amendment dated 2-13-92, at 9-11, ‘602 patent.” (6/13/03 MOSAID App. at p. 2).

The intrinsic evidence clearly supports MOSAID’s admission that capacitor boosting circuits and double bootstrapping circuits were disclaimed by the patentee. During prosecution of the application that issued as the ‘602 patent, the patentee distinguished her invention from the prior art reference Tran on the basis that Tran uses a capacitor boosting circuit. Appl. No. 07/680,746, 2/13/92 Response to PTO Action at p. 9. In Tran, the capacitor boosting circuit is a capacitor connected to the word line that provides an unregulated, boosted voltage to the word line. *Id.* at 7-9. The patentee differentiated her invention by arguing that the Lines invention applies a controlled voltage to the word line without using a capacitor boosting

¹⁵If this disclaimer is applicable to the claim term “means for applying,” it will also apply to six other, related claim terms found in the Lines patents:

- 1) “applying circuitry” (‘640 patent, claim 1);
- 2) “applying the controlled high voltage V_{pp} to the word line” (‘640 patent, claim 1);
- 3) “from one of the latched, level shifted control signals applying a controlled high voltage, from the controlled high voltage supply, to a selected word line” (‘253 patent, claim 31);
- 4) “from one of the latched, level shifted control signals applying a controlled high voltage greater than the stored voltage to a selected word line” (‘643 patent, claim 15);
- 5) “from the latched, level shifted control signals, applying a controlled voltage to the selected word line” (‘643 patent, claim 28); and
- 6) “applies the controlled high voltage V_{pp} from the high voltage supply to a word line” (‘253 patent, claim 15).

circuit. *See, e.g., Id.* at 10 (“In [Tran,] it is the boosted capacitor voltage, *not the supply voltage* as defined in applicant’s claims 1-3 . . . which is applied to the word line.”) (emphasis in original). Thus, the patentee disclaimed the use of capacitor boosting circuits connected to the word line.

The patentee also disclaimed the use of double bootstrapping circuits. MOSAID asserts that the ordinary meaning of a “double bootstrapping circuit” is a boosting capacitor that provides an unregulated voltage to the drain of a self-bootstrapping N-MOS transistor.¹⁶ Defendants on the other hand contend that a double bootstrapping circuit is nothing more than a circuit that boosts an already boosted voltage, *i.e.*, it creates a double boosted voltage.

The Court finds that the ordinary meaning of double bootstrapping can be ascertained from the intrinsic evidence. All of the Lines patents derive priority from a foreign application. A portion of that foreign application was filed with the U.S. Patent & Trademark Office during prosecution of Application No. 07/680,746, a patent application all of the Lines patents originate from. That portion of the foreign application addresses what the patentee considered to be double bootstrapping:

The gate of the pass device is driven high by the wordline to connect the storage capacitor to the bitline. In order for a V_{dd} bit line potential to be stored on the capacitor the wordline must be driven to a voltage above $V_{dd} + V_{in}$. Word-line driver circuitry left over from the days of NMOS DRAM makes use of n-channel devices only. The gate of the n-channel wordline driver output device must be driven to a voltage significantly greater than $V_{dd} +$

¹⁶If the Court were to adopt MOSAID’s proposed ordinary meaning of a “double bootstrapping circuit,” and conclude that the patentee disclaimed its use, by MOSAID’s own admission, such a disclaimer would amount to nothing since no one currently makes DRAM chips that use a boosting capacitor in conjunction with a self-bootstrapping transistor to drive the word line. (1/30/04 *Markman* Tr. at 206:12-18).

$2V_m$ to allow sufficient drive in achieving $> V_{dd} + V_m$ on the wordline within a reasonable length of time. The technique of capacitive coupling gate voltage boosting produces the so-called double-bootstrapped voltage. In small geometry VLSI processes these high voltages can exceed reliability limits. Appl. No. 07/680,746, 6/24/91 Letter Claiming Right of Priority, UK Appl. No. 9007790 (emphasis added).

Further, the '602 specification discusses the prior art and the serious problems that occurred when using an N-MOS transistor as a pass transistor:

During the early days of DRAM design, *NMOS type FETs, that is, N-channel devices were used exclusively*. In order to pass a $V_{dd} + V_{tn}$ level signal to the selected word line, the gate of the pass transistor had to be driven to at least $V_{dd} + 2V_{tn}$. Furthermore, to allow sufficient drive to achieve a voltage greater than $V_{dd} + V_{tn}$ on the word line within a reasonable length of time in order to facilitate a relatively fast memory, *the gate of the pass transistor is driven to a significantly higher voltage*. In such devices, the word line driving signal utilized capacitors in a well-known double-bootstrap circuit.

In the above circuit, *the boot strapping voltage circuit is designed to exceed the voltage $V_{dd} + 2V_{tn}$* , in order to ensure that temperature, power supply, and process variations would never allow the pass transistor driving voltage to fall below $V_{dd} + 2V_{tn}$.

However, it has been found that in small geometry VLSI memories, *the high voltages provided by the boot-strap circuits can exceed the tolerable voltages in the memory*, thus adversely affecting reliability. '602 col. 1, ll. 28-54 (emphasis added).

The '602 specification goes on to explain how the Lines inventions improved upon the flaws of the prior art:

The present invention is a circuit which accurately controls the word line (*pass transistor gate*) driving voltage to a voltage which is both controlled and is not significantly greater than is needed to drive the word line. The elements of the present invention *eliminate the need for a double-boot-strapping circuit, and ensure that no voltages exceed that necessary to fully turn on a memory cell access transistor*. Accordingly, voltages in excess of that which would reduce reliability are avoided, and accurate driving

voltages are obtained. '602 patent, Abstract and '602 col. 1, ll. 56-65 (emphasis added).

* * *

Thus, an above V_{dd} voltage level on the word line is achieved *without the use of double boot-strap circuits*. '602 patent, Abstract (emphasis added).

As those sections make clear, using an N-MOS transistor as the pass transistor causes problems because in order to pass a full boosted voltage (*e.g.*, $V_{dd} + V_{tn}$) to the word line, the voltage on the gate has to be driven to a significantly higher voltage (*e.g.*, greater than $V_{dd} + 2V_{tn}$). The patentee referred to this technique as “capacitive coupling gate voltage boosting,” which produces the double bootstrapped voltage. Even though that technique includes the word “capacitive,” it does not appear that an actual capacitor is required to create the double bootstrapped voltage, as MOSAID contends. As MOSAID’s expert explained, a self-bootstrapping transistor is a transistor that uses its own *internal capacitance* to raise its gate voltage and allow “the full voltage at its drain to pass to its source without a threshold voltage drop.” (Greene Expert Report at ¶ 16). Thus, the “double bootstrapped voltage” appears to be nothing other than the voltage generated at the gate of a self-bootstrapping N-MOS transistor when passing an already boosted voltage to the word line.

The Lines patents sought to overcome this problem by using a P-MOS transistor as the pass transistor instead of an N-MOS transistor. Since a P-MOS transistor requires zero volts on the gate to pass the full boosted voltage to the word line, it does not require the application of higher boosted voltages that give rise to the reliability problems. The patentee articulated her solution to this problem in the prosecution history:

There are *three components to this invention*, a high voltage V_{pp} supply, a word line driver *utilizing a p-channel pass device between wordline and boosted precoded address*, and a boosted address predecoder utilizing a V_{pp} supply. *Together they eliminate the need for double-boot-strapping* and ensure that no voltages exceed that necessary to fully turn on a memory cell access transistor. Appl. No. 07/680,746, 6/24/91 Letter Claiming Right of Priority, UK Appl. No. 9007790 (emphasis added).

Accordingly, the intrinsic evidence clearly conveys that the patentee disclaimed double bootstrapping circuits, *i.e.*, a self-bootstrapping N-MOS transistor as the pass transistor.

Consequently, the “means for applying” shall include a disclaimer that it must perform that function without double bootstrapping.

MOSAID musters one last argument based on the doctrine of claim differentiation why a self-bootstrapping N-MOS transistor should not be excluded from the scope of the term “means for applying.” MOSAID argues that independent claim 31 of the ‘253 patent must be given a broader construction, and may include an N-MOS transistor as the pass transistor, because dependent claim 35 requires the use of a P-MOS transistor as the pass transistor. Although the doctrine of claim differentiation creates a presumption that the two claims are different in scope, that presumption “can not broaden claims beyond their correct scope.” *Kraft Foods, Inc. v. Int’l Trading Co.*, 203 F.3d 1362, 1368 (Fed. Cir. 2000) (citation omitted). In this case, that presumption cannot overcome the patentee’s clear disclaimer of double bootstrapping. *Fantasy Sports Props., Inc. v. SportsLine.com, Inc.*, 287 F.3d 1108, 1115-16 (Fed. Cir. 2002) (finding the presumption of claim differentiation was overcome by the patentee’s disclaimer of subject matter in the prosecution history). Thus, claim 31, and any other independent claim that

does not recite the type of transistor used to apply the high voltage to the word line, cannot correctly read on a double bootstrapping circuit.

Finally, regarding Defendants' contention that the inventors disclaimed the use of voltages that exceed V_{pp} in the entire DRAM chip, the Court disagrees. Although the specification does discuss "ensur[ing] that no voltages exceed that necessary to fully turn on a memory cell access transistor," '602 patent, col. 1, ll. 61-63, it only makes that reference in regards to the voltages applied to the pass transistor and the memory cell access transistor. *See* '602 patent, col. 1, ll. 33-65. Nowhere in the specification or prosecution history does it require that voltages in the entire DRAM chip not exceed V_{pp} and, therefore, this alleged disclaimer does not apply to the term "means for applying."¹⁷

3. "directly"

The parties dispute the ordinary meaning of the word "directly." Claim 1 of the '602 patent states in pertinent part: "means . . . for applying the V_{pp} supply voltage level *directly* to the word line through the source-drain circuit of an FET." '620 patent, claim 1 (emphasis added). Defendants argue that "directly" means that the FET must apply the voltage to the word line without any intervening circuitry. MOSAID argues that "directly" does not exclude intervening circuitry as long as the voltage level does not change between the FET and the word line.

¹⁷The parties agree to the meaning of the claim term " V_{pp} ," but disagree as to whether it is subject to the disclaimer that it is the highest voltage used in the DRAM chip. For the reasons stated above, this disclaimer does not apply. Thus, the term " V_{pp} " means "a substantially constant high supply voltage at or higher than V_{dd} plus a transistor threshold voltage." (1/27/04 Chart entitled "Agreed and Partially Agreed Claim Terms" at p. 2).

The Court begins its analysis by looking to the language of the claims. The claim language is clear on its face that a voltage level is applied directly through a FET to the word line. Based on that clear language, the word “directly” and its context demonstrate that there simply is no room for intervening circuitry. MOSAID’s construction would not only read the word “directly” out of the claim, but the words “to” and “through” as well. As a result, the ordinary meaning of “directly” is “without intervening circuitry.”

The dictionary definitions submitted by the parties support that ordinary meaning of the claim term. The definition of “directly” is “in a direct way or line; straight . . . without a person or thing coming between; immediately.” *Webster’s New World Dict.* 399 (2d ed. 1980). Two other dictionary definitions of “directly” were also provided by the parties:

1a: without any intervening space or time: next in order:
SQUARELY, EXACTLY

* * *

2c: without divergence from the source of the original

Webster’s Third New Int’l Dict. 641 (1986). Defendants contend that all three of the definitions support an ordinary meaning of “a direct line . . . without anything or anyone intervening.” MOSAID does not address the first two definitions. Instead, MOSAID asserts that the ordinary meaning of “directly” is definition 2c above – “without divergence from the source of the original.”

The Court agrees with Defendants and finds that the ordinary meaning does not allow for any intervening circuitry. Even if the Court adopted definition 2c above as the ordinary meaning, it still would not change the plain meaning of the claim. “[W]ithout divergence from

the source of the original” connotes a straight line between two points without branching off on a different course. MOSAID’s interpretation of that definition would effectively require this Court to rewrite the term “directly” as “without changing the voltage level.” Although the patentee could have acted as her own lexicographer, she did not. It is not the Court’s obligation to rewrite the claims to reflect what the patentee may have been able to claim, but to ascertain the ordinary meaning of the claim language she did in fact use.

The intrinsic evidence does not alter the ordinary meaning of “directly.” During prosecution of the ‘602 patent application, the patentee added the word “directly” to distinguish the Lines invention from a prior art reference that included a capacitor between the pass transistor and the word line. The patentee explained the purpose of adding the word “directly” by stating:

In order to distinguish even more clearly, applicant has added the word “directly” in line 14 of claim 1, thus specifying even more clearly that the voltage supply level is applied “directly” to the word line through the source drain circuit of an FET.

* * *

The applicant claims in claim 7, and in all of the other claims, an invention which provides a word line voltage that does not include a capacitor type bootstrap circuit and applies that voltage directly from a power supply. Appl. No. 07/680,746, 2/13/92 Response to PTO Action at pp. 11, 15.

MOSAID claims that those remarks were an attempt to distinguish a prior art reference that used circuitry to boost the supply voltage before it was applied to the word line. Thus, according to MOSAID, the word “directly” was added to emphasize that the voltage level being applied to the word line remains unchanged from the voltage level leaving the FET.

MOSAID's position is unconvincing. Those remarks were made to distinguish the Lines invention from a reference that had a circuit between the pass transistor and the word line. The patentee clarified that the word "directly" was added to demonstrate that there was no intervening circuitry, such as a capacitor, between the pass transistor and the word line. This is evident from another remark made by the patentee earlier in that same response:

Contrast this with applicant's invention as shown in Figure 1. *The voltage to be applied to the word line is received from a power supply at a desired voltage V_{pp} directly through transistor 14A.* The word line is switched between ground and V_{pp} by means of transistors 13A and 14A. There is no slow-charging bootstrap circuit required. There is no capacitor connected to the word line which must be charged to provide the word line voltage in a bootstrap circuit, and as shown in both Figures 2 and 3 of Tran. Appl. No. 07/680,746, 2/13/92 Response to PTO Action at p. 10 (emphasis added, underline in original).

Accordingly, "directly" means "without any intervening circuitry."

4. "connected/coupled"

Although the parties agree that "connected" and "coupled" have the same meaning, they dispute whether those terms require that electrical components be connected without intervening circuitry. MOSAID contends that "connected" may include intervening circuitry; the Defendants contend that "connected" requires that there be no intervening circuitry.

The analysis begins by ascertaining the ordinary meaning of the disputed term. Both parties submit dictionary definitions that allegedly support their proposed claim construction. Defendants submit the following dictionary definitions for "connected:"

“1. united, joined, or linked. 2. having a connection. 3. joined together in sequence;” *The Random House Dict. of the English Language* 431 (2d ed. 1987).

“1. conjoined; fastened or linked together.” *The Oxford English Dict.* 745 (2d ed. 1989).

MOSAID defines “connect” as “to join, fasten, or link together usually by something intervening.” *Webster’s Third New Int’l Dict.* 480 (1986). MOSAID latches onto the phrase “something intervening” and extracts from it that two items may be connected if any number of components intervene. However, contrary to MOSAID’s assertion, the Court does not believe that this dictionary definition supports MOSAID’s open-ended construction. Instead, the definition uses “something intervening” to describe the means by which two things are joined, fastened or linked together. For example, two items may be connected if they are physically joined, *e.g.*, the halves of a ziploc bag pressed together, or if they are fastened together by something intervening, *e.g.*, a memory cell access transistor connected to a bit line by a wire. *See* ‘602 patent, Fig. 1. In fact, the dictionary even provides an example of two items that are connected by something intervening – “a bus line connects the two towns.” *Webster’s Third New Int’l Dict.* at 480.

Nothing in MOSAID’s definition suggests that two items may be considered connected if there are any number of intervening components. Taken to an extreme, MOSAID’s interpretation of “connected” would mean that every electrical component on a DRAM chip is connected to all the other components no matter how many millions of intervening components there are. That interpretation does not coincide with the ordinary meaning of the term.

Consequently, the ordinary meaning of the term “connected” is “united, joined, or linked together.”

Next, one looks to the intrinsic evidence to see if “connected” takes on a meaning that is different than its ordinary meaning. Claim 1 of the ‘602 patent includes the following pertinent language:

[M]emory cells *connected* to the bit lines and word lines, each memory cell being comprised of an access field effect transistor (FET) having its source-drain *connected* between a bit line and a high logic level voltage V_{dd} bit charge storage capacitor, the field effect transistor having a gate *connected* to a corresponding word line ‘602 patent, claim 1 (emphasis added).

Looking at Figure 1 of the ‘602 patent, it is clear that the claim consistently uses the term “connected” to mean that components are linked together without any intervening circuitry, a fact that MOSAID does not dispute.

The specification of the Lines and Foss patents supports the ordinary meaning of “connected.” For example, in the Lines specification, the patentee states:

The output of NAND gate is *connected through* an inverter 9 to the gate of an N-channel FET 10. FET 10 has its source *connected* to ground and its drain *connected* to control node 8A. ‘602 patent, col. 2, ll. 51-54 (emphasis added).

In the second sentence, it is clear that “connected” was used to mean without any intervening circuitry. Indeed, the first sentence shows that when there was intervening circuitry, the patentee would use the phrase “connected through.” The Foss specification also uses “connected” in a consistent manner:

With reference to FIG. 3, a capacitor 15 is *connected* in a series circuit between ground and *through* an N-channel field effect transistor 16, configured as a diode, with gate and drain *connected*

to a voltage source V_{dd} . '620 patent, col. 3, ll. 35-38 (emphasis added).

MOSAID contends that a broader interpretation of “connected” is warranted by how it is used in claim 1 of the '620 patent. According to MOSAID, '620 claim 1 uses the term “connected” to mean “through intervening components.” MOSAID focuses on the portion of claim 1 that states “the switching circuit alternately *connecting* the first terminal of the boosting capacitor to the voltage supply and to the capacitive load.” '620 patent, claim 1 (emphasis added). MOSAID asserts that if one looks at the embodiment set forth in Figure 3 of the '620 patent, the switching circuit connects the right side of boosting capacitor 27 to the voltage supply through transistor 23, and connects the right side of boosting capacitor 27 to the output terminal 19 through transistor 24. Thus, argues MOSAID, the boosting capacitor is connected through intervening circuitry, and if the Court adopts Defendants' narrow construction of without intervening circuitry, '620 claim 1 would not cover the preferred embodiment depicted in Figure 3.

Although MOSAID's argument may appear to be correct at first, upon closer inspection it simply does not hold up. Contrary to MOSAID's assertion, claim 1 of the '620 patent clearly supports defining “connected” as directly linked when the excerpt that MOSAID focuses on is looked at in the appropriate context. Claim 1 states in relevant part:

[A] switching circuit including a *first switch* between one level of the voltage supply and the first terminal of the boosting capacitor and a *second switch* between the first terminal of the boosting capacitor and a capacitive load, the first and second switches being driven by clock signals, the switching circuit *alternatively connecting the first terminal of the boosting capacitor to the voltage supply and to the capacitive load*. '620 patent, claim 1 (emphasis added).

Focusing on the relationship between the boosting capacitor and the voltage source, it is clear that the claim does not state that they are connected. In fact, the plain meaning of “alternately connecting” is that unless the switching circuit performs the act of connecting, the two components are normally disconnected. If the Court were to adopt MOSAID’s construction, however, it would turn the plain meaning of the claim on its head because “electronically connected with or without intervening components” would mean that the boosting capacitor and voltage source are always connected. If they are always connected, the requirement that the switching circuit alternately connect them would be meaningless and the Foss pump would be inoperative. Accordingly, MOSAID’s definition is inconsistent with the plain language of the claim.

Contrary to MOSAID’s assertion, when the ordinary meaning of the term “connected” is used in ‘620 claim 1, the claim includes the embodiment set forth in Figure 3. The claim clearly states that the *switching circuit* connects the boosting capacitor to the voltage source. Inserting the ordinary meaning of “connects” into the claim, it would read that the switching circuit, *i.e.*, a first switch or transistor 23, directly links the boosting capacitor to the voltage source without any intervening circuitry. That is exactly what Figure 3 depicts. Thus, adopting a construction that excludes intervening circuitry does not exclude the embodiment depicted in Figure 3.

The remainder of the intrinsic evidence does nothing to evince a different understanding of the term “connected.” Accordingly, based on the ordinary meaning and plain language of the patent claims, the terms “connected” and “coupled” shall be construed as meaning “directly united, joined, or linked together.”

5. “means for receiving”

The parties agree that this claim term should be construed as a means-plus-function term pursuant to 35 U.S.C. § 112 ¶ 6. The parties also agree that the “means for receiving” performs the function of “receiving V_{dd} level logic inputs and providing an output to the applying means at V_{pp} logic levels.” *See* ‘602 patent, claim 2. The parties, however, do not agree on the structure that performs that function.

MOSAID argues that NAND gate 5 performs the claimed function. MOSAID’s construction however contains a fundamental flaw – the NAND gate 5 does not provide an output at V_{pp} logic levels. Attempting to circumvent this problem, MOSAID contends that the claimed function does not require the “means for receiving” to provide an output at V_{pp} logic levels. Instead, MOSAID argues, the function requires that the “means for receiving” provide an output to the applying means, and the applying means be at V_{pp} logic levels.

MOSAID’s position is incorrect. The phrase “at V_{pp} logic levels” in the agreed upon function does not modify the “applying means;” it modifies “an output.” Thus, the output of the “means for receiving” must be “at V_{pp} logic levels.” With this basic understanding, it becomes blatantly obvious that NAND gate 5 cannot perform this function.

Defendants seize upon the fundamental flaw in MOSAID’s proposed structure to suggest that the structure must include level shifter 6 in addition to NAND gate 5. However, Defendants position is flawed for a different reason – level shifter 6 cannot be a part of the “means for receiving.” As the function of the “means for receiving” indicates, it is separate and apart from the means for applying. The means for applying, as previously construed by the Court and agreed to by Defendants, includes level shifter 6 as part of its structure. *See* Section 2 *supra*;

see also '602 patent, claim 3 (identifying level shifter 6 as part of the applying means). Since level shifter 6 is a part of the means for applying, it cannot be a part of the "means for receiving" and, therefore, Defendants proposed structure is incorrect.

"As the quid pro quo for the convenience of employing § 112, paragraph 6, [the patentee] has a duty to clearly link or associate structure to the claimed function." *Budde v. Harley-Davidson, Inc.*, 250 F.3d 1369, 1377 (Fed. Cir. 2001) (citation omitted). "[F]ailure to disclose adequate structure corresponding to the recited function in accordance with 35 U.S.C. § 112 paragraph 1, results in the claim being of indefinite scope, and thus invalid, under 35 U.S.C. § 112, paragraph 2." *Id.* at 1376 (citation omitted). If one of skill in the art were to try to determine the boundaries of claim 2 of the '602 patent, they would be unable to because the patentee did not identify any structure that can perform the claimed function. Consequently, claim 2 of the '602 patent is invalid as indefinite. Additionally, since claims 3 and 4 of the '602 patent depend on claim 2, and thus also include the "means for receiving" limitation, those claims are invalid as indefinite as well.

6. "level shifter driving means"

This claim term is found in claim 3 of the '602 patent. As stated above, this claim is invalid because it includes the indefinite term "means for receiving." However, even if that is not the case, claim 3 is still invalid as indefinite due to the term "level shifter driving means."

The parties agree that the disputed term is a means-plus-function claim term. They also agree to a claimed function: "driving the level shifter." *See* '602 patent, claim 3. However, just like the "means for receiving" term, the issue is whether the specification

identifies any structure that can perform the claimed function. The “level shifter driving means” limitation is found in claim 3 of the ‘602 patent, which describes where the structure should be located:

A DRAM as defined in claim 2 in which the applying means is comprised of a level shifter connected to said high supply voltage source having an output connected to the gate of a pass transistor whose source is connected to said high supply voltage source, said word line and *level shifter driving means* being connected *between the level shifter and ground*, the level shifter driving means being *connected to the output of the selecting means*. ‘602 patent, claim 3 (emphasis added).

MOSAID recognizes that the claim language places the structure between NAND gate 5 and the level shifter. Even though Figure 1 and the specification of the ‘602 patent do not identify any structure at that location, MOSAID attempts to salvage the claim by asserting that the structure is transistors 10 and 11. Further, MOSAID asserts that transistors 10 and 11 receive an output from the NAND gate and drive the level shifter, which it contends is limited to transistors 7A and 7B. Defendants counter by arguing that there is no disclosed structure that performs the claimed function and thus claim 3 is indefinite.

There is no support for MOSAID’s proposed structure in the ‘602 specification. Transistors 10 and 11 cannot be the structure that drives the level shifter because they are in fact identified as part of the level shifter. ‘602 patent, col. 2, line 46 (identifying Box 6 as the level shifter, which in Figure 1 includes transistors 10 and 11). MOSAID fails to identify any part of the specification that defines the level shifter differently or limits it to transistors 7A and 7B. Consequently, MOSAID’s proposed structure must be rejected.

In short, the '602 patent does not identify any structure located between NAND gate 5 and level shifter 6 that could be the "level shifter driving means." Consequently, claim 3 and dependent claim 4 of the '602 patent are invalid as indefinite.

7. "word line driver circuit"

The parties dispute whether the "word line driver circuit" can provide a driving voltage to a word line or a group of word lines.

Defendants assert that there can only be one word line for each word line driver circuit. Defendants contend that the ordinary meaning of the term "word line driver circuit" indicates that it is limited to a single word line. Defendants rely on MOSAID's definition of "driver" to support this alleged ordinary meaning. "Driver" is defined as "[a]n electronic circuit that supplies input to another electronic circuit." *IEEE Standard Dict. of Electrical and Electronics Terms* 291 (4th ed. 1988). Defendants argue that this definition supports their construction that a "word line driver circuit" supplies an input (*i.e.*, voltage) to a word line.

Although Defendants are correct that this definition supports their construction, the Court finds that this definition is also consistent with MOSAID's broader construction. Nothing in the definition limits a driver to supplying an input to only one circuit. On the contrary, it appears that a circuit that applied an input to multiple circuits would still be a driver. Since the Court is required to "give a claim term the *full range* of its ordinary meaning as

understood by persons skilled in the relevant art,”¹⁸ the ordinary meaning of “word line driver circuit” will include “one or more word lines.”

Next, the Court turns to the claim language to determine whether the ordinary meaning is consistent with the claims. The phrase “word line driver circuit” is found in multiple claims in the ‘253 and ‘643 patents. The ‘253 patent is representative of how the term is used:

- ! “a word line driver circuit which applies the controlled high voltage V_{pp} from the high voltage supply *to a word line*” ‘253 patent, claim 15 (emphasis added);
- ! “a word line driver circuit which applies the controlled voltage from the voltage supply *to a word line*” ‘253 patent, claim 22 (emphasis added);
- ! “a word line driver circuit, which applies the controlled high voltage V_{pp} from the V_{pp} supply *to a selected word line*” ‘253 patent, claim 29 (emphasis added).

Defendants contend that these relevant excerpts demonstrate that a “word line driver circuit” applies a voltage to a *single* word line. MOSAID counters by arguing that the word “a” before “word line” means one or more and thus the “word line driver circuit” is not limited to *only* one word line.

MOSAID has the better argument. The word “a” in the ‘253 claims does not limit the word line driver circuit to only one word line. *See KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000) (“This court has repeatedly emphasized that an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more’ in open-ended claims construing the transitional phrase ‘comprising.’”) (citations omitted). Since the claims do not

¹⁸*Texas Digital Sys., Inc. v. Telegenix, Inc.*, 308 F.3d 1193, 1202 (Fed. Cir. 2002) (emphasis added, citation omitted).

require that the “word line driver circuit” work with only one word line, its plain and ordinary meaning includes one or more word lines.

Defendants contend that the broader meaning of “word line driver circuit” is not supported by the specification. Defendants argue that nothing in the Lines patents states or even hints at the possibility that the word line driver can drive more than one word line. Defendants argue that one of ordinary skill in the art reading the Lines patents would believe that a secondary decoder’s only function would be as an alternative voltage source for that one word line. Thus, according to Defendants, the “word line driver circuit” would be limited to the embodiment shown in Figure 1 of the Lines patents.

For the reasons stated above under the “means for applying” section, see Section 2 *supra*, Defendants’ arguments are unconvincing. The secondary decoder is clearly contemplated as a circuit that can be used in conjunction with the “word line driver circuit” to select and drive more than one word line. Accordingly, the specification does not limit the ordinary meaning of “word line driver circuit” to the embodiment set forth in Figure 1 of the Lines patents.

In sum, the plain and ordinary meaning of “word line driver circuit” is unambiguous and means “a circuit that applies a driving input voltage to a single word line or a group of word lines.”¹⁹

¹⁹This construction determines how the Court construes the disputed claim terms “word line selection signals” (‘253, ‘640 and ‘643 patent claims), “select signals” (‘253 claim 29), “word line control signals” (‘253, ‘640 and ‘643 patent claims) and “control signals” (‘253 and ‘643 patent claims). The only dispute between the parties concerning these terms is whether they are limited to a single word line or could apply to a group of word lines. Having found that the Lines invention contemplated an embodiment including a group of word lines, the Court adopts MOSAID’s proposed constructions for each of those claim terms.

8. “latching level shifter”

Having agreed to the meaning of “level shifter,” the parties dispute what the word “latching” means in this claim term. A “level shifter” has been defined as “a circuit that accepts digital input signals at one pair of voltage levels and delivers output signals at a different pair of voltage levels, where at least one of those voltage levels changes.” (1/27/04 Chart entitled “Agreed and Partially Agree Claim Terms” at p. 4). Defendants contend that a “latching level shifter” is a level shifter that will retain at least one state, *i.e.*, will continue to provide an output signal, in the absence of input signals. MOSAID on the other hand contends that a “latching level shifter” holds the output signals *only* while the input signals are present. If MOSAID’s construction is adopted, a “latching level shifter” without input signals would not provide any output signals.

The Court begins by trying to determine the ordinary meaning of the claim language. Claim 15 of the ‘253 patent states in relevant part: “a *latching* level shifter which receives word line selection signals at V_{dd} logic levels *to* drive and *latch* first and second word line control signals at V_{pp} logic levels.” ‘253 patent, claim 15 (emphasis added). Thus, it appears that the terms “latching” and “latch” are being used in a technical sense.

Defendants proffer the Radio Shack dictionary definition of “latch,” which is “[a] feedback loop used in a symmetrical digital circuit (such as a flip-flop) to retain a state.” *Radio Shack Dict. of Electronics* (5th ed. 1977). MOSAID criticizes this definition, arguing that the definition does not support Defendants’ proposed construction because the definition requires a “symmetrical circuit,” whereas Defendants’ construction would define “latching” as an asymmetrical circuit since it only needs to retain one state. However, MOSAID does not dispute

that the ordinary meaning of the technical word “latch” includes the ability to retain at least one state. In fact, MOSAID’s own expert submitted an expert report in support of its claim construction that states: “Generally, a ‘latch’ is understood to refer to a circuit that retains its output state in the absence of inputs.” (Greene Expert Report at ¶ 18). Consequently, the ordinary meaning of “latching” means “retaining an output state in the absence of inputs.”

MOSAID maintains that this definition cannot be correct because it is inconsistent with, and in fact would exclude, the “latching level shifter” set forth in Figure 1 of the patents. The level shifter in Figure 1 is not a symmetrical “latching level shifter.” It can only retain one output state in the absence of input signals, an output of V_{pp} from transistor 7A to the gate of pass transistor 14A, which would not allow any voltage to pass to the word line. In order for it to be a symmetrical “latching level shifter,” it would need an additional pull-down transistor, like transistor 12, to be connected to the gate of transistor gate 7A. Since it lacks that additional pull-down transistor, MOSAID argues that it cannot be a “latching level shifter” as defined by the Radio Shack dictionary. Thus, MOSAID offers an alternative definition of “to . . . latch” which is “to hold the output signals while the input signals are present.”

There are several problems with MOSAID’s analysis and proffered claim construction. First, as explained above, the ordinary meaning of “latch” only requires that an output state be retained, not that the circuit be symmetrical and be able to retain multiple outputs. Thus, the ordinary meaning would include the level shifter embodied in Figure 1. Second, even if the ordinary meaning of “latch” required a symmetrical circuit, the Court would conclude that the patentee acted as her own lexicographer and broadened the meaning so that it only required one output state to be retained based on Figure 1.

Finally, MOSAID's proffered claim construction cannot be correct because it would strip the terms "latching" and "latch" of any meaning. There is nothing to suggest, and MOSAID offers no evidence, that NAND gate 5 will provide constant input signals to the level shifter so that it becomes "latched." As a result, there is no evidence that the "latching level shifter" would ever "latch" any signals if MOSAID's definition were adopted.

The patentee purposefully used the terms "latching" and "latch" in a technical manner and it is the Court's responsibility to give effect to those words. Since Defendants' proposed construction would give meaning to the disputed terms and would include the preferred embodiment Figure 1, the Court finds that a "latching level shifter" is "a level shifter including a feedback loop that will indefinitely retain at least one data state in the absence of any new control signal to change the state."²⁰ *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998) ("The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction.").

²⁰The parties agree that the claim terms "level shifter with latching" ('643 claim 1; '640 claim 1), "latching the level shifted control signals" ('253 claim 31; '643 claims 15 and 28) and "to latch" ('253 claims 15, 22 and 29; '643 claim 1; '640 claim 1) are terms related to "latching level shifter" and thus should be construed consistently. Having concluded that a "latching level shifter" requires the level shifter to be able to retain at least one state without input signals, the Court adopts Defendants' proposed claim constructions for those related terms.

9. “DC voltage supply”

Defendants contend that “DC voltage supply” is the “external supply voltage V_{dd} .” MOSAID counters by arguing that Defendants’ construction is far too limited because nothing in the ‘620 patent requires that it be limited to an external supply voltage or to the voltage V_{dd} .

The plain language of the claim term must be considered in the context of the claim that it arises. Claim 1 of the ‘620 patent is representative of the use of that term and states:

A random access memory comprising:

DC voltage supply providing plural voltage levels;

a boosting capacitor having first and second terminals;

switching circuit including a first switch between one level of the voltage supply and the first terminal of the boosting capacitor and a second switch between the first terminal of the boosting capacitor and a capacitive load, the first and second switches being driven by clock signals, the switching circuit alternately connecting the first terminal of the boosting capacitor to the voltage supply and to the capacitive load while alternating the level of the voltage supply connected to the second terminal of the boosting capacitor to pump the voltage on the capacitive load to a boosted voltage level greater than and of the same polarity as the DC voltage supply;

a feedback loop responsive to the boosted voltage level to control the switching circuit to regulate the boosted voltage to a substantially static value greater in magnitude than the voltage levels of the DC voltage supply and of a correct level required to turn on a selected memory cell access transistor; and

a decoder circuit supplying the regulated boosted voltage to a word line and the gate of the memory cell access transistor to store a voltage on a storage capacitor of the memory. ‘620 patent, claim 1.

Defendants do not dispute that this plain language is not limited to an external voltage or to a voltage V_{dd} . Instead, they assert that the ordinary meaning of “DC voltage supply” supports their construction.

Defendants provide dictionary definitions for the phrase “supply voltage.”

MOSAID contends that these definitions are inapt because “voltage supply” and “supply voltage” are two separate and distinct concepts in the art of DRAM chips. However, as Defendants point out, the ‘620 specification uses the terms interchangeably, see ‘620 patent, col. 1, ll. 27-31; col. 1, l. 63 - col. 2, l. 2; col. 3, ll. 49-53; col. 5, ll. 23-25; col. 5, ll. 62-64, and thus the Court will consider these definitions as informative of the ordinary meaning of the phrase “DC voltage supply.”

The first definition of “supply voltage” is “[t]he voltage, usually direct, applied by an external source to the circuit of an electrode.” *IEEE Standard Dict. of Electrical and Electronics Terms* 968 (4th ed. 1988). The dictionary definition for “direct current (dc) supply voltage” is “[t]he mean value of the direct voltage between the input terminals, taken over one period of the ripple voltage appearing between the input terminals.” *Id.* at 270. In order to further understand that definition, Defendants assert that one of skill would look to the definition of the word “terminal” set forth in that dictionary, which is defined as “[a]n externally available point of connection to one or more electrodes or elements within the device.” *Id.* at 997. Thus, argue Defendants, the ordinary meaning of “direct current (dc) supply voltage” would inform one that it is referring to the direct voltage applied to the externally available points of connection.

Defendants then seize on the word external in the “supply voltage” and “direct current (dc) supply voltage” definitions, and argue that it means “external to the DRAM chip.”

However, those definitions are not that restrictive. “External” in those definitions could mean external to a circuit, *e.g.*, pass transistor 14A, not necessarily external to the entire DRAM chip. Nothing in those definitions requires a supply voltage to be external to the DRAM chip. Thus, the Court gives the ordinary meaning of “DC voltage supply” its full range and finds that it includes both internal and external voltages.

Defendants argue that the patentees considered “DC voltage supply” to be synonymous with V_{dd} . As proof, Defendants cite to the prosecution history of the ‘620 patent where the patentees used the phrases “the main DC supply V_{dd} ” and “the DC voltage supply (V_{dd}).” Appl. No. 09/483,626, 10/31/00 Response to PTO Action at p. 4. However, those phrases are not indicative of a clear disavowal of scope for “DC voltage supply.” Instead, they were used when discussing the embodiment set forth in Figure 3 of the Foss patents. *Id.* at 3-4. As a result, they simply show that in Figure 3 of the patent, the “DC voltage supply” is equal to V_{dd} .

Further, nothing in the ordinary meaning or intrinsic evidence requires that “DC voltage supply” be limited to V_{dd} voltage levels. The plain meaning of the claims suggests that the “DC voltage supply” may provide “plural voltage levels.” ‘620 patent, claim 1. Although this may include V_{dd} voltage levels, the plain meaning does not require that it be limited to V_{dd} . Indeed, if the patentees wanted to limit “DC voltage supply” to V_{dd} , they could have simply used the term V_{dd} . But the patentees purposefully used the term “DC voltage supply,” and absent some clear indication that it was meant to be limited to V_{dd} , the Court will not find it so limited.

Accordingly, the plain and ordinary meaning of the term “DC voltage supply” is “a supply that provides two or more substantially constant output voltages.”²¹

10. “switching circuit alternately connecting”

The parties agree to a construction for this claim term with one exception.

Defendants define “switching circuit alternately connecting” as “*alternately* connecting the first terminal of the boosting capacitor at one time to the voltage supply and at a different time to the capacitive load.” (Emphasis added). In lieu of the word “alternately,” MOSAID proposes that the word “repetitively” be used. Thus, the dispute reduces to one of whether an “alternately connecting” circuit must “alternately connect” or “repetitively connect.” The answer is obvious.

The plain language of the claim term – “switching circuit alternately connecting” – resolves the dispute. The term itself uses the word “alternately,” not repetitively. Further, neither the claim term nor the claim itself includes the word “repetitively” or requires that the switching circuit repetitively connect. Therefore, consistent with the plain language of the claim, the term will be defined using the word “alternately.”

Defendants also assert that the claim term should be subject to a disclaimer that the switching circuit, *i.e.*, the Foss pump, work “without double bootstrapping.” Defendants support their argument with references to the intrinsic evidence of the Foss patents.²² In

²¹The parties agree that the term “voltage supply” (‘620 patent) is related to “DC voltage supply” and thus should be resolved in an identical manner. Accordingly, “voltage supply” means “a supply that provides two or more substantially constant output voltages.”

²²The disclaimer of double bootstrapping discussed earlier concerning the claim term “means for applying” was done so in the context of the Lines patents. Since this claim term is located in the Foss patents, not the Lines patents, the disclaimer of double bootstrapping must

particular, the Defendants point to the prosecution history of the Foss patents, where the patentees described their invention as follows:

Advantages

1. Accurate regulation of boosted word line potential
2. Save CV^{**2}/T power dissipation
3. Improved reliability - *this technique eliminates double bootstrap voltages on the chip*
4. High efficiency - pump can approach an output

Appl. No. 07/680,994, 10/4/91 Letter Claiming Right of Priority, UK Appl. No. 9007791.8 at p. 1 (emphasis added). These were described as advantages over the prior art DRAM chips that “typically use[d] a capacitive voltage boosting technique to drive the wordline.” *Id.* In other words, one of the advantages of the Foss patents is the elimination of double bootstrap voltages created by the word line driver circuitry. This disclaimer did not exclude the use of circuits that generate double bootstrap voltages within the Foss pump.

The Defendants’ citations to the specification buttress that understanding. In every Foss patent, the patentees discussed the elimination of double bootstrapping in the same manner:

Since the voltage that is exactly that required is generated, improved reliability is achieved because double boot-strap voltages on the chip are eliminated. ‘620 patent, col 2, ll. 47-50.

* * *

The voltage regulator described above thus eliminates the boosting of V_{pp} if it is not required, and only allows the voltage boosting circuit to boost the voltage to the level required by the word line, i.e. cell access transistors. This saves power and provides protection to the cell access transistors, increasing reliability of the memory. The dangerous double boot-strap circuits boosting

once again be addressed.

voltage to about $2V_{dd}$ which were previously found on the chip are thus eliminated, and voltage stress is minimized. '620 patent, col. 6, ll. 38-41.

Although those excerpts speak of eliminating double bootstrap voltages, they do so in the context of the word line driver circuitry, not the Foss pump. One of the main advantages of the Foss pump is its ability to create an output voltage "as high as $2V_{dd}$." '620 patent, col. 2, ll. 14-17. If those excerpts disclaimed double bootstrapping in the Foss pump as Defendants suggest, then the Foss pump would eliminate the creation of double bootstrap voltages, *i.e.*, voltages of about $2V_{dd}$. Clearly, this cannot be the case. It would not make any sense for the Foss invention to simultaneously permit generating voltages as high as $2V_{dd}$, while preventing voltages of the same magnitude because they create reliability problems.

Consequently, although the Court agrees with Defendants that the patentees disclaimed double bootstrapping, the Court does not agree that they did so in the context of the Foss pump. As discussed previously, double bootstrapping circuits were problematic and created reliability problems when they were used *as part of the word line driver to pass the voltage onto the word line*. However, the patents do not discuss, and the parties do not point to, any statements that clearly disclaim the use of double bootstrapping *within the Foss pump*.

In order to understand this distinction, it is important to keep in mind the difference between the Lines word line driver and the Foss pump. The Lines word line driver is concerned with applying a regulated, boosted voltage to the word line. In order to perform that function, the patentee disclaimed the use of a boosting capacitor attached to the word line because it created unregulated voltages and the use of an N-MOS transistor as the pass transistor because it created the dangerous double bootstrap voltages.

The Foss pump on the other hand is not concerned with using regulated voltages or avoiding double boosted voltages *within the pump*. Instead, its sole purpose is to produce a regulated, boosted voltage that can be used by the Lines word line driver circuit. Regardless of what circuits are used in the Foss pump, the output should always be a regulated, boosted voltage. And, as the '620 specification makes clear, it is this regulated, boosted voltage that makes the elimination of dangerous double bootstrap voltages possible:

Thus accurate regulation of the boosted word line voltage is produced, without the danger of transistor damaging voltages. Because once the word line driving voltage is reached, the voltage pump is inhibited, there is no additional power required to charge voltage boosting capacitors higher than this point, saving power. Since the voltage that is exactly that required is generated, improved reliability is achieved because double boot-strap voltages on the chip are eliminated. The circuit is thus of high efficiency. '620 patent, col. 2, ll. 41-49.

Accordingly, “switching circuit alternately connecting” is not subject to the disclaimer “without double bootstrapping.”²³

11. “switching circuit . . . alternating the level”

Related to the previous “switching circuit alternately connecting” dispute, the parties dispute whether a “switching circuit . . . alternating the level” should mean a switching

²³The parties agree that the term “alternately switching” ('620 claim 13; '201 claim 11; '581 claims 5 and 14) is related to “switching circuit alternately connecting” and should be resolved in the same manner. The parties dispute whether the proper construction of the term should begin with the word “alternately” or “repetitively,” and also dispute whether it is subject to a disclaimer of “without double bootstrapping.” For those reasons articulated above, the Court finds that “alternately switching” means “alternately switching the first terminal of the boosting capacitor at one time to the voltage supply and at a different time to the capacitive load,” and that the disclaimer does not apply.

circuit that is *alternately* or *repetitively* “connecting the second terminal of the boosting capacitor at one time to a low level of the DC voltage supply and at a different time to a high level of the DC voltage supply.” As articulated above, the word “alternately” is more appropriate because it is consistent with the plain language of the claims. Thus, the construction of “switching circuit ... alternating the level” shall include “alternately.”

Defendants raise a new disclaimer argument concerning this claim term. The Defendants contend that the Foss patents disclaim the use of clock sources to charge the boosting capacitor.²⁴ The patentees allegedly disclaimed the use of clock sources in the “Detailed Description of the Invention” when they distinguished their invention from the prior art based on what voltage source is used to charge the boosting capacitor.

It should be noted that the capacitors 15, 22 and 27 charge from the main voltage supply V_{dd} , and not from the clock sources. This allows the clock sources to have reduced power supply requirements, since they drive only the gates of the FETs which have minimal capacitance. This is in contrast to the prior art boosting circuit in which the clock sources supply the charge required for capacitors 9 and 11 (Fig. 1), and thus supply the current required to boost the voltage, indirectly supplying part of the word line current. ‘620 patent, col. 5, ll. 23-31 (emphasis added).

Defendants contend that having distinguished the Foss pump from the prior art, the patentees evinced a clear disavowal of claim scope that must be given effect.

²⁴Defendants also argue that the patentees disclaimed the use of an inverter as a circuit that connects the input terminals of the boosting capacitor to different voltage levels. However, unlike their argument concerning the use of clock sources, there is nothing in the specification that even suggests that the patentees meant for their invention to exclude the use of an inverter. It may be that an inverter could only be used in a Foss pump to permit clock sources to charge the boosting capacitor. In that case, the disclaimer regarding clock sources resolves the issue. But to the extent an inverter can be used in the Foss pump for some other purpose, there has been no disavowal of claim scope.

MOSAID accuses Defendants of trying to deviate from the ordinary meaning of “alternating the level” by importing a limitation from the specification into the claim term. According to MOSAID, the ordinary meaning of the claim term would include the use of clock sources as voltage sources. MOSAID contends that Defendants mischaracterize the excerpt from the Foss specifications as a clear disavowal of claim scope. That excerpt, MOSAID asserts, merely recites an advantage of the preferred embodiment of the Foss patents.

Defendants’ contention is more likely correct. Although a Court may not read limitations from the specification into the claims, “[w]here the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the claims of the patent, even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass the feature in question.” *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001).

In this situation, the specification clearly conveys to one of ordinary skill in the art that the use of clock sources to charge the boosting capacitor is not covered by the Foss patents. First, the “Abstract” of the Foss patents explicitly state that the inventions eliminate the problems associated with using clock sources as the voltage supply: “The boosting capacitors are charged by V_{dd} , thus eliminating drift tracking problems associated with clock boosting sources and V_{dd} .” ‘620 patent, Abstract. Second, the excerpt quoted above by the Defendants did more than discuss an advantage of the Foss invention; it clearly distinguishes the Foss invention from the prior art. Notably, that distinction between the Foss invention and the prior art was set forth in a section titled, “Detailed Description of the Invention.” ‘620 patent, col. 3, ll. 32-33. Although the section title itself may not be deserving of great weight, it is deserving of some because

patentees have other nomenclature at their disposal and will instead often include a section entitled, "Description of a Preferred Embodiment of the Invention." *See, e.g.*, '602 patent, col. 2, ll. 17-18. The patentees of the Foss patents on the other hand purposefully chose to characterize that section as a description of their invention. Lastly, as MOSAID admitted during the *Markman* hearing, the Foss patents only describe an embodiment where the boosting capacitor charges from the voltage supply. (1/30/04 *Markman* Tr. at 321:14-16).

In summary, there is no indication that the use of clock sources to charge the boosting capacitor was simply an advantage of a preferred embodiment. Accordingly, the Court finds that the Foss patents disclaimed the use of the clock sources to charge the boosting capacitor.

12. "correct level required to turn on a selected memory cell access transistor"

Claims 1 and 13 of the '620 patent contain the "correct level" claim limitation. Claim 1 of the '620 patent is representative and states in relevant part: "a feedback loop . . . to regulate the boosted voltage to a substantially static value . . . of a correct level required to turn on a selected memory cell access transistor." '620 patent, claim 1.

Defendants contend that "correct level" should be construed to mean the lowest voltage necessary to turn on a memory cell access transistor. MOSAID, on the other hand, contends that "correct level" is any voltage level greater than or equal to the lowest voltage necessary to turn on the access transistor so long as that voltage level will not cause damage to the access transistor. Thus, the dispute as framed by the parties is whether the "correct level" is

limited to the lowest voltage necessary to turn on an access transistor, or includes higher voltages that are less than transistor damaging voltages.

Defendants assert that the ordinary meaning of the word “required” supports their claim construction. The word “require” is defined as “to have as a requisite; need,”²⁵ “to demand as necessary or essential: have a compelling need for,”²⁶ and “to have need of; need.”²⁷ Recognizing that the word “necessary” is common to all of those dictionary definitions, Defendants conclude that “[t]he voltage level that is ‘required to turn on’ the access transistor is the *minimum* voltage that is necessary.” (Infineon Br. at 59).

Defendants’ conclusion is wrong. None of the Defendants’ dictionary definitions include the word “minimum.” The ordinary meaning of “required” is “necessary,” not “the minimum necessary.” And if the ordinary meaning of “required” is used, the voltage level that is “required” to turn on an access transistor is a voltage level that is “necessary” to turn on the access transistor. A voltage level that is necessary to turn on the access transistor can be the lowest voltage necessary, but it can also be a higher voltage that does not damage the transistor.

The claim language supports the broader construction of “correct level.” When the claim term is viewed in the context of the claim, as this Court is required to do, it is clear that the “correct level” voltage is a boosted voltage of a “substantially static value.” ‘620 patent, claim 1. A “substantially static value” is obviously not a static value and, thus, the plain language of the claims indicate that the voltage level may have some amount of variation.

²⁵*Am. Heritage Dict.* (Microsoft bookshelf CD-ROM) (2d Collegiate ed. 1987).

²⁶*Webster’s Ninth New Collegiate Dict.* 1002 (1990).

²⁷*The Random House Dict. of the English Language* 1636 (2d ed. 1987).

Regardless of the amount of variation, the fact that the claims indicate that there may be some amount undermines Defendants' contention that "correct level" must be limited to "the lowest voltage necessary," *i.e.*, only one voltage.

Further, the claims require the voltage to be of "a" correct level. The use of the word "a" indicates that the "correct level" may be one or more voltages, not just a single voltage. *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000). Accordingly, the ordinary and plain meaning of the "correct level" claim term is "a voltage level sufficient to fully turn on a memory cell access transistor but not so high that it will damage the transistor."²⁸

Defendants also contend that the patentees acted as their own lexicographers and defined the "correct level" by limiting it to the lowest voltage necessary to turn on the access transistor. After reviewing the written description, the Court disagrees. Although the patentees did describe an embodiment where the word line voltage is brought to the "exact word line supply voltage, neither too low nor too high,"²⁹ that was a description of a specific, preferred embodiment, not all embodiments. '620 patent, col. 2, ll. 25-51. The '620 claims buttress that conclusion because that specific embodiment is not required by all of the claims. *Compare* '620 claim 1 *with* dependent claim 10. Accordingly, the patentees did not limit the meaning of "correct level" in the Foss specifications and, thus, the ordinary and plain meaning governs.

²⁸Defendants argued at the *Markman* hearing that if MOSAID's construction is adopted, the term is indefinite because one of ordinary skill in the art would not know what a transistor damaging voltage is. Defendants' argument is not well received because it agreed with MOSAID that the definition of "transistor damaging voltage" is "a voltage that instantaneously causes the gate oxide to rupture." (1/27/04 Chart entitled "Agreed and Partially Agreed Claim Terms" at p. 5). Thus, one of skill in the art would understand what range of voltages the "correct level" falls between and accordingly Defendants' indefiniteness argument must fail.

²⁹'620 patent, col. 6, ll. 44-45.

13. “decoder circuit”

The “decoder circuit” limitation is set forth in claim 1 of the ‘620 patent. Claim 1 states in pertinent part:

[A] decoder circuit supplying the regulated boosted voltage to a word line and the gate of the memory cell access transistor to store a voltage on a storage capacitor of the memory.
‘620 patent, claim 1.

Although the parties agree that the “decoder circuit” is “a circuit that decodes word line address information,” it is clear from the plain language of the claim that the decoder circuit does more than that. Not only does the “decoder circuit” decode address information, it also supplies the regulated boosted voltage to a word line. Thus, the Court finds that a “decoder circuit” is “a circuit that decodes word line address information and supplies the regulated boosted voltage to the word line.”

The sole remaining issue is whether a “decoder circuit” performs its function “without using double bootstrapping to store a voltage on a memory cell storage capacitor.” As discussed above with regards to the claim term “switching circuit alternately connecting,” see Section 10 *supra*, the Foss patents did not disclaim the use of double bootstrapping within the Foss pump. Instead, they disclaimed the use of double bootstrapping to apply a voltage to the word line. *See, e.g.*, ‘602 patent, col. 2, ll. 47-50 and col. 6, ll. 38-41. Since the ordinary meaning of “decoder circuit” shows that it supplies the boosted voltage to the word line, the disclaimer applies.³⁰

³⁰The parties agree and the Court finds that the term “word line decoder” (‘201 patent, claim 1) is related to “decoder circuit” and, therefore, construes it in an identical manner.

14. “switching means”

The parties dispute whether “switching means” is a means-plus-function limitation governed by 35 U.S.C. § 112 ¶ 6. MOSAID acknowledges, as it must, that the claim term includes the word “means” and, therefore, is presumptively a means-plus-function limitation. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1369 (Fed. Cir. 2002). But MOSAID argues that this presumption is rebutted for one of two reasons: 1) the term itself is structural, and 2) even if it is not structural, the claim recites sufficient structure for the identified functions. Defendants on the other hand argue that this term is a means-plus-function limitation because it is not a structural term and fails to recite sufficient structure for *each* function identified in the claims.

MOSAID argues that the term “switching” is structural in nature. MOSAID asserts that even if “switching” does not call to mind any particular structure to one of ordinary skill in the art, as long as it imparts structure of some fashion it is sufficient to rebut the means-plus-function presumption. (1/5/04 MOSAID Opp. Br. at p. 47). According to MOSAID, a “switching means” is structural because it means a circuit or apparatus that employs switches.

MOSAID cites to three cases where claim terms including the word “means” were found not to be means-plus-function limitations because, in addition to the structure recited for performing the claimed functions, the terms themselves were structural in nature. *Cole v. Kimberly-Clark Corp.*, 102 F.3d 524, 530-31 (Fed. Cir. 1996) (construing the term “perforation means”); *Envirco Corp. v. Clestra Cleanroom, Inc.*, 209 F.3d 1360, 1364-65 (Fed. Cir. 2000) (construing the term “baffle means”); *General Creation LLC v. Leapfrog Enters., Inc.*, 232 F. Supp. 2d 661, 671-73 (W.D. Va. 2002) (construing the term “switch means”). In each of those

cases, the court found that the term, *e.g.*, perforation, baffle and switch, possessed an ordinary meaning that imparted structure and thus rebutted the presumption that § 112 ¶ 6 applies.

In this case, however, the word “switching” is not structural in nature; it is a verb that expresses action. In fact, one of MOSAID’s cases distinguished between “switch means,” which it considered structural, and “switching means,” which it stated “was clearly in means-plus-function format.” *Leapfrog Enterprises*, 232 F. Supp. 2d at 673; *see also Overhead Door Corp. v. Chamberlain Group, Inc.*, 194 F.3d 1261, 1271 (Fed. Cir. 1999) (finding that “first switch means” and “memory selection second switch means” were properly considered by the district court to be means-plus-function limitations).

Further, MOSAID has failed to carry its burden of showing that the ordinary meaning of the term “switching” is structural in nature. In sharp contrast to the cases that MOSAID cites to, where the parties submitted dictionary definitions to show that the ordinary meaning of the word contained structure, MOSAID fails to submit a dictionary definition showing that the word “switching” is structural. Instead, MOSAID asserts through attorney argument that the ordinary meaning of “switching means” is a circuit or apparatus that employs switches. Accordingly, MOSAID’s argument that “switching means” is itself structure is insufficient to overcome the presumption of § 112 ¶ 6.

MOSAID also contends that “switching means” is not a means-plus-function limitation because the claim recites sufficient structure to perform the claimed function. In order to determine the function or functions of the claim term “switching means,” the particular claim language must be examined. Claim 1 of the ‘201 patent, which includes the claim term “switching means,” recites in relevant part:

[S]*witching means* including a first switch between one level of the voltage supply and the first terminal of the boosting capacitor and a second switch between the first terminal of the boosting capacitor and a capacitive load, the first and second switches being driven by clock signals, the *switching means alternately connecting* the first terminal of the boosting capacitor to the voltage supply and to the capacitive load *while alternating the level* of the voltage supply connected to the second terminal of the boosting capacitor to pump the voltage on the capacitive load to a boosted voltage level greater than and of the same polarity as the DC voltage supply to provide a boosted voltage supply. ‘201 patent, claim 1 (emphasis added).

MOSAID contends that the claimed function is “to pump the voltage on the capacitive load to a boosted voltage level greater than and of the same polarity as the DC voltage supply.”³¹

MOSAID then relies on this function to argue that sufficient structure is identified in the claim to rebut the means-plus-function presumption.

MOSAID’s asserted function misconstrues the plain claim language. MOSAID’s identified function is not a function, but a result of the functions that the “switching means” performs. Claim 1 of the ‘201 patent requires the “switching means” to perform two different functions. First, it “alternately connect[s] the first terminal of the boosting capacitor to the voltage supply and to the capacitive load.” ‘620 patent, claim 1. Second, it “alternat[es] the level of the voltage supply connected to the second terminal of the boosting capacitor.” *Id.* When the switching circuit performs these two functions, the result is that the voltage level in the capacitive load is boosted higher. *See, e.g.*, ‘201 patent, col. 4, l. 51 - col. 5, l. 9.

Having identified the claimed functions, the Court must then identify the corresponding structure for each of those functions. *Budde v. Harley-Davidson, Inc.*, 250 F.3d

³¹Originally, MOSAID identified the claimed function as including “alternately connecting the first terminal of the boosting capacitor to the voltage supply and to the capacitive load.” (7/18/03 MOSAID’s Reply Exh. A at p. 15). MOSAID never revealed to this Court why it discarded that function for its current, proposed function.

1369, 1376 (Fed. Cir. 2001); *Epcon Gas Sys., Inc. v. Bauer Compressors, Inc.*, 279 F.3d 1022, 1033 (Fed. Cir. 2002) (“The district court did not err in requiring that ‘corresponding structure’ include at least that structure necessary to perform each of the functions recited as being performed by the ‘control means’ in claim 16.”). Although the claim does recite structure that corresponds to the first function of “alternately connecting,” *i.e.*, the first and second switches, the claim does not recite any structure for the second function of “alternating the [voltage] level.” This lack of structure confirms that “switching means” is indeed a means-plus-function limitation, and requires the Court to look to the specification to identify corresponding structure.

“Structure disclosed in the specification is ‘corresponding’ structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim.” *B. Braun Med., Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997). The parties agree that the structure for the first function includes transistors 23 and 24, and the structure for the second function includes 25 and 26.³² Defendants, however, also contend that the clock signals, *e.g.*, ϕ_1^+ and ϕ_2^+ , that drive those transistors are corresponding structure. MOSAID disagrees and argues that clock signals are voltage levels and, therefore, cannot be corresponding structure. MOSAID has the better argument. The clock signals are clearly voltage levels that are applied to the gates of the transistors. *See, e.g.*, ‘201 patent, col. 4, ll. 8-11. Therefore, the structure identified by the written description corresponding to the first function is transistors 23 and 24, and the structure corresponding to the second function is transistors 25 and 26.

³²The Court agrees that these transistors are corresponding structure as recited by the written description of the ‘201 patent. ‘201 patent, Fig. 3 and col. 3, l. 35 - col. 5, l. 49.

Lastly, the Defendants argue that the patentees disclaimed the use of clock sources to charge the boosting capacitor in the “switching means.” The disclaimer of clock sources to charge the boosting capacitor was discussed earlier in the context of the ‘620 patent. *See* Section 11 *supra*. Since the ‘201 patent is related to the ‘620 patent, having issued from an application that was a continuation of the ‘620 application, its specification is materially identical to the ‘620 specification. *Applied Materials, Inc. v. Advanced Semiconductor Materials Am., Inc.*, 98 F.3d 1563, 1579 (Fed. Cir. 1996) (Mayer, J., concurring) (“By definition, a continuation adds no new matter and is akin to an amendment of a pending application.”). Accordingly, for the same reasons articulated above that found a disclaimer applies, the same disclaimer “without using clock sources to charge the boosting capacitor” applies to “switching means.”

CONCLUSION

The disputed claim terms have the following meanings:

1. “ V_{dd} ” means “the substantially constant positive source-drain supply voltage in a MOS circuit.”
2. “means for applying” is a means-plus-function limitation. Its function is “applying the V_{pp} supply voltage level directly to the word line through the source-drain circuit of an FET.” Its corresponding structure includes “level shifter 6 and transistor 14A or level shifter 6, transistor 14A and a secondary decoder.” Further, the patentee disclaimed the use of a double bootstrapping circuit and a capacitor boosting circuit.
3. “applying circuitry” means “circuitry that applies without using a double bootstrapping circuit or a capacitor boosting circuit.”

4. “applying the controlled high voltage V_{pp} to the word line” means “putting on the controlled voltage V_{pp} to the word line through the source drain circuit of a pass FET without using a double bootstrapping circuit or a capacitor boosting circuit.”

5. “from one of the latched, level shifted control signals applying a controlled high voltage, from the controlled high voltage supply, to a selected word line” means “to put on a controlled high voltage, from the controlled high voltage supply, to a selected word line without using a double bootstrapping circuit or a capacitor boosting circuit.”

6. “from one of the latched, level shifted control signals applying a controlled high voltage greater than the stored voltage to a selected word line” means “to put on a controlled high voltage greater than the stored voltage to a selected word line without using a double bootstrapping circuit or a capacitor boosting circuit.”

7. “from the latched, level shifted controls signals, applying a controlled voltage to the selected word line” means “to put on a controlled voltage to the selected word line without using a double bootstrapping circuit or a capacitor boosting circuit.”

8. “applies the controlled high voltage V_{pp} from the high voltage supply to a word line” means “to put on the controlled high voltage V_{pp} from the high voltage supply to a word line without using a double bootstrapping circuit or a capacitor boosting circuit.”

9. “ V_{pp} ” means “a substantially constant high supply voltage at or higher than V_{dd} plus a transistor threshold voltage.”

10. “directly” means “without any intervening circuitry.”

11. “connected” and “coupled” mean “directly united, joined, or linked together.”

12. “means for receiving” is indefinite. As a result, the Court finds that claims 2, 3 and 4 of the ‘602 patent are invalid as indefinite pursuant to 35 U.S.C. § 112 ¶¶ 2 and 6.

13. “level shifter driving means” is indefinite. As a result, the Court finds that claims 3 and 4 of the ‘602 patent are invalid as indefinite pursuant to 35 U.S.C. § 112 ¶¶ 2 and 6.

14. “word line driver circuit” means “a circuit that applies a driving input voltage to a single word line or a group of word lines.”

15. “word line selection signals” means “signals derived from address information that select a single word line or a group of word lines.”

16. “select signals” means “signals derived from address information that select a single word line or a group of word lines.”

17. “word line control signals” means “signals used to control the application of a voltage to a single word line or a group of word lines.”

18. “control signals” means “signals used to control the application of a voltage to a single word line or a group of word lines.”

19. “latching level shifter” means “a level shifter including a feedback loop that will indefinitely retain at least one data state in the absence of any new control signal to change the state.”

20. “level shifter with latching” means “a level shifter including a feedback loop that will indefinitely retain at least one data state in the absence of any new control signal to change the state.”

21. “latching the level shifted control signals” means “using a feedback loop to store and retain the boosted states of the control signals.”

22. “to . . . latch” means “to indefinitely retain at least one data state with a feedback loop in the absence of any new control signal to change the state.”

23. “DC voltage supply” means “a supply that provides two or more substantially constant output voltages.”

24. “switching circuit alternately connecting” means “alternately connecting the first terminal of the boosting capacitor at one time to the voltage supply and at a different time to the capacitive load.”

25. “alternately switching” means “alternately switching the first terminal of the boosting capacitor at one time to the voltage supply and at a different time to the capacitive load.”

26. “switching circuit . . . alternating the level” means “alternately connecting the second terminal of the boosting capacitor at one time to a low level of the DC voltage supply and at a different time to a high level of the DC voltage supply without the use of clock sources to charge the boosting capacitor.”

27. “correct level required to turn on a selected memory cell access transistor” means “a voltage level sufficient to fully turn on a memory cell access transistor but not so high that it will damage the transistor.”

28. “decoder circuit” means “a circuit that decodes word line address information and supplies the regulated boosted voltage to the word line without using double bootstrapping.”

29. “word line decoder” means “a circuit that decodes word line address information and supplies the regulated boosted voltage to the word line without using double bootstrapping.”

30. “switching means” is a means-plus-function limitation. Its functions are: “1) alternately connecting the first terminal of the boosting capacitor to the voltage supply and to the capacitive load; and 2) alternating the level of the voltage supply connected to the second terminal of the boosting capacitor.” Its corresponding structure includes: “1) transistors 23 and 24; and 2) transistors 25 and 26.”

The agreed upon claim terms have the following meanings:

31. “high V_{pp} supply voltage source” means “a circuit that generates V_{pp} .”
32. “controlled high voltage V_{pp} supply” means “a circuit that generates V_{pp} .”
33. “controlled high voltage supply” means “a circuit that generates a substantially constant high supply voltage.”
34. “a high voltage supply which supplies a controlled high voltage V_{pp} ” means “a circuit that generates V_{pp} .”
35. “a voltage supply which supplies a controlled voltage” means “a circuit that generates a substantially constant supply voltage.”
36. “ V_{dd} logic levels” means “logic levels in which the high level is V_{dd} .”
37. “ V_{pp} logic levels” means “logic levels in which the high level is V_{pp} .”
38. “decoding address signals” means “producing output signals based on input address signals.”
39. “switch” means “a device for making, breaking, or changing the connection of a circuit, but not a transistor introducing a threshold voltage drop or a transistor configured as a diode.”

40. “boosted clock signal” means “a clock signal that has been boosted above the high level of the DC voltage supply.”

41. “boosted voltage level” means “a voltage level that has been boosted above the high level of the DC voltage supply.”

42. “unregulated boosted voltage” means “a boosted voltage level that is not controlled.”

43. “level shifter” means “a circuit that accepts digital input signals at one pair of voltage levels and delivers output signals at a different pair of voltage levels, where at least one of those voltage levels changes.”

44. “control signals being set and reset” means “control signals being placed in a zero or one state by only V_{dd} level signals.”

45. “dynamic random access memory” means “a dynamic form of random access memory that uses, as its memory storage elements, capacitors that are built into the integrated circuit; the data stored on the capacitors requiring periodic refreshing.”

46. “random access memory” means “a memory that permits access to any of its address locations in any desired sequence with similar access time to each location.”

47. “means for selecting” is a means-plus-function claim limitation. Its function is “selecting the word line.” Its structure is “NAND gate 5.”

48. “high logic level voltage V_{dd} bit charge storage capacitor” means “a bit charge storage capacitor that stores a high logic level voltage V_{dd} .”

49. “transistor threshold voltage / threshold voltage” means “the minimum voltage between the gate and source of a MOS transistor at which the channel begins to conduct current.”

50. “P-channel FET / p-channel transistor” means “a field effect transistor where source and drain are regions of p-type conductivity, and holes are used to conduct current in the channel region.”

51. “N-channel FET / n-channel transistor” means “a field effect transistor where source and drain are regions of n-type conductivity, and electrons are used to conduct current in the channel region.”

52. “transistor damaging voltage” means “a voltage that instantaneously causes the gate oxide to rupture.”

An appropriate order will be entered.

Dated: March 23, 2004

S/William J. Martini

William J. Martini, U.S.D.J.

cc: Clerk of the Court
The Honorable Ronald J. Hedges, U.S.M.J.